SECTION 1 MECHANIZED LOOP TESTING (MLT) OVERVIEW

In This Section:

1.1. SYSTEM OVERIVEW

POTS Test Assurance Program (**PTAP**) is a process that incorporates Training in Mechanized Loop Testing (**MLT**) Architecture and Operation, Analysis of Testability Problems, and Problem Resolution Techniques.

LoopCare™, owned by Tollgrade Communications, Inc., provides a single, comprehensive, test system for telecommunications network operators and is capable of analyzing both metallic and digital loop testing.

1.2. PTAP – Course Objectives

The purpose of PTAP training is to provide sound, overall understanding of MLT, thereby providing students with the technical knowledge necessary to troubleshoot and resolve MLT testing problems in the Central Office (**CO**) and Digital LoopCare™ (**DLC**) systems. Also, PTAP provides instructions in the proper installation and use of Tollgrade MCU® products, which will enable the student to maintain a high level of testability on all direct and DLC—fed loops.

1.3. Automated Test System

Mechanized Loop Testing (**MLT**) provides automated testing and analysis of telephone lines and equipment across a broad range of services including Plain Old Telephone Service (**POTS**), Digital Loop Carrier (**DLC**), and the Integrated Services Digital Network (**ISDN**). MLT functionalities include the following:

- Automated test system
- Performs tests on—demand, or pro—active (Program Scan, Automatic Line

Insulation Test (ALIT)

- Analyzes problems in CO, outside plant and CPE
- Can perform rapid and interactive tests
- Provides **VER Codes** to permit automated screening.

1.4. TEST PATHS FOR POTS, INTEGRATED AND UNIVERSAL TESTING

Figure 1•1 is an example of test paths for POTS, Integrated and Universal Testing.

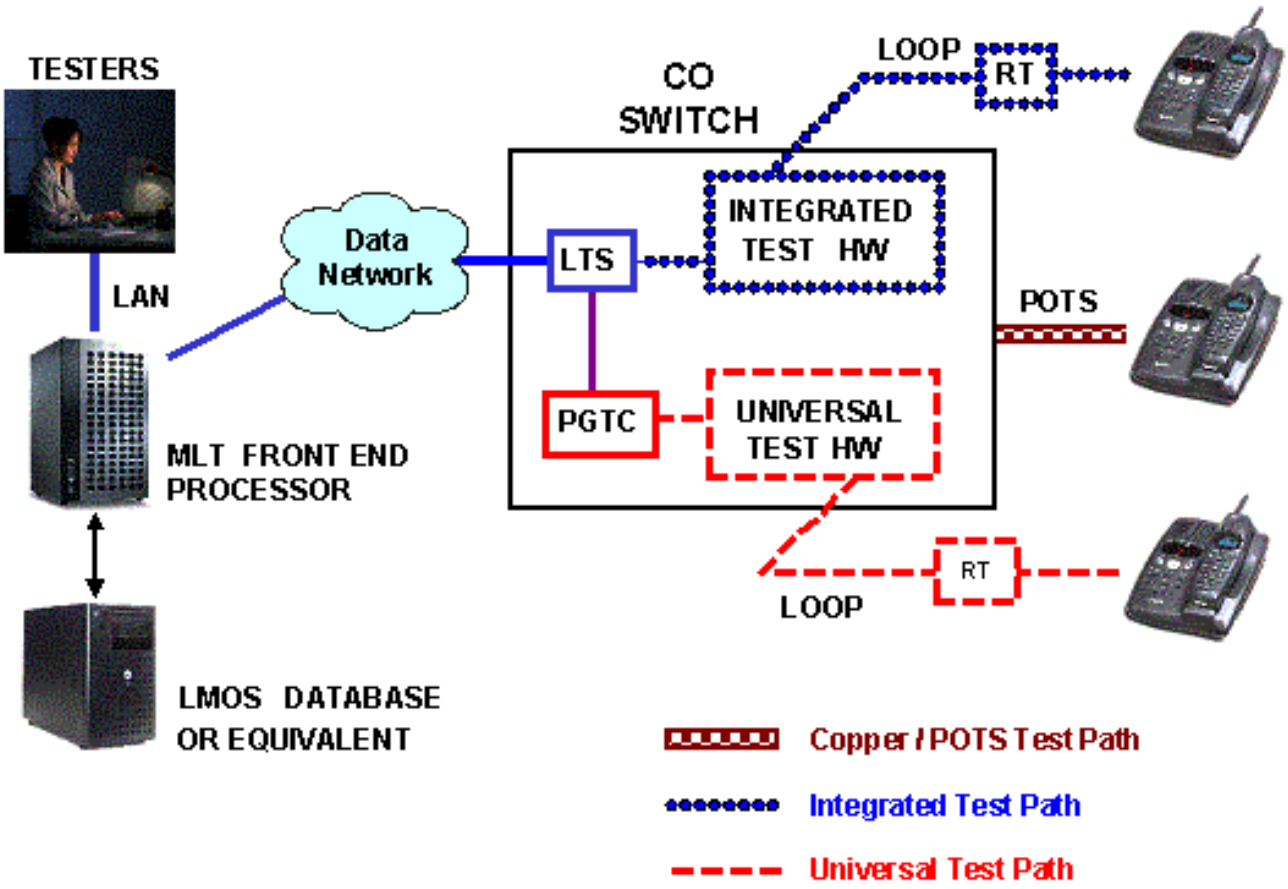


Figure 1•1 Test Paths for POTS, Integrated, and Universal Testing

1.5. MLT architecture

- Application Software — Resides in transaction processor
- Operating System/Database — Loop Maintenance Operating System (**LMOS**) or equivalent
- Local Area Network (**LAN**) — Connects testers to processor
- Data Communications Network (**DCN**) — Connects processor to test hardware
- Test hardware consists of the following components:
    - o Loop Test System (**LTS**) — For testing POTS
    - o Pair Gain Test Controller (**PGTC**) — Provides for universal system testing
    - o Directly Connected Test Unit (**DCTU**) — Replaces the LTS and is integrated into the 5ESS (**IMLT**)
    - o Test Bus Control Unit (**TBCU**) — Provides for Integrated testing on 5ESS switch
    - o Metallic Test Access (**MTA**) — Provides for integrated testing on DMS—100 switch
    - o Digital Line Unit (**DLU**) — Provides for integrated testing on Siemens (**EWSD**) switch.

1.6. MLT Testing Metallic, Universal, AND

Integrated Systems

MLT testing for metallic, universal, and integrated systems includes the following:

- Mechanized Loop Testing • Basic Metallic Loop Testing
- Universal DLC Testing
- Integrated DLC Testing • 5ESS
- Integrated DLC Testing • 5ESS/IMLT (**DCTU**)
- Integrated DLC Testing – DMS•100
- Integrated DLC Testing – EWSD.

1.7. Basic Metallic Loop Testing

The following diagrams are examples of test paths for POTS, integrated, and universal testing.

Figure 1•2 is an example of Basic Metallic Loop Testing.

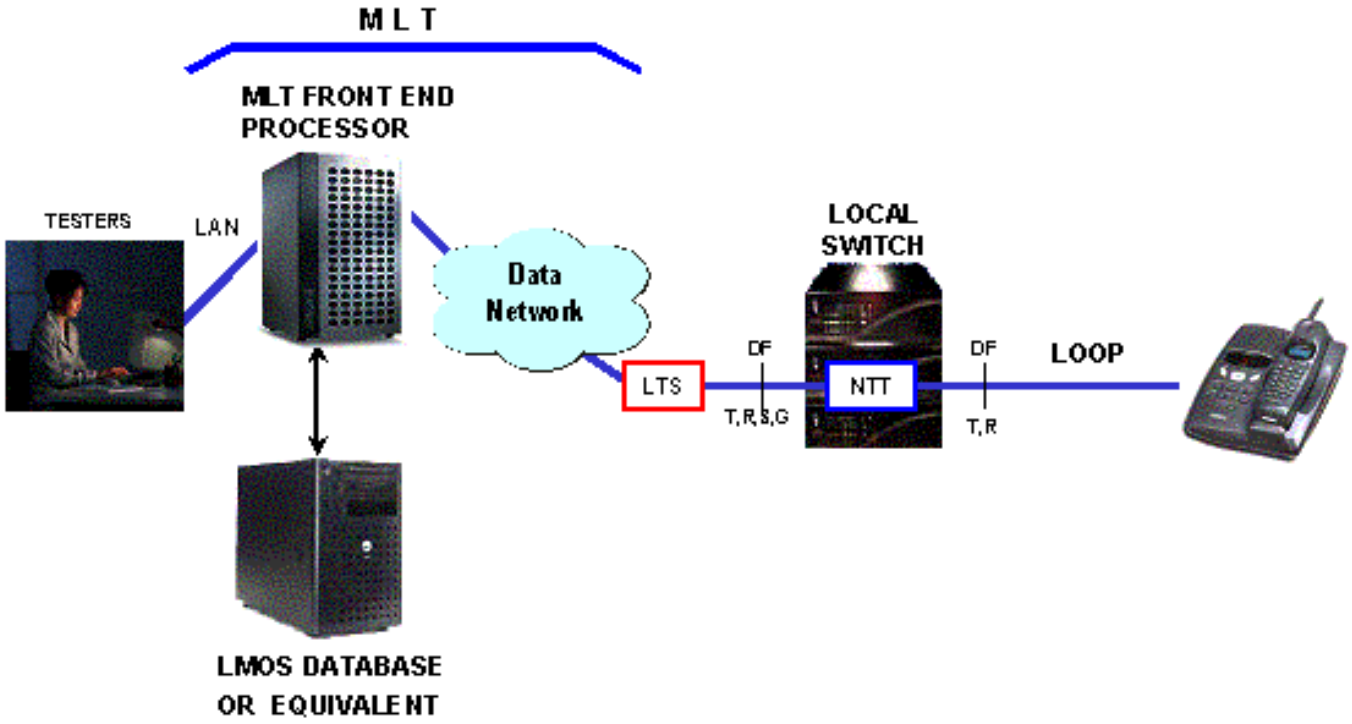


Figure 1•2 Basic Metallic Loop Testing

1.8. Universal DLC Testing

Figure 1•3 is an example of Universal DLC (**UDLC**) Testing.

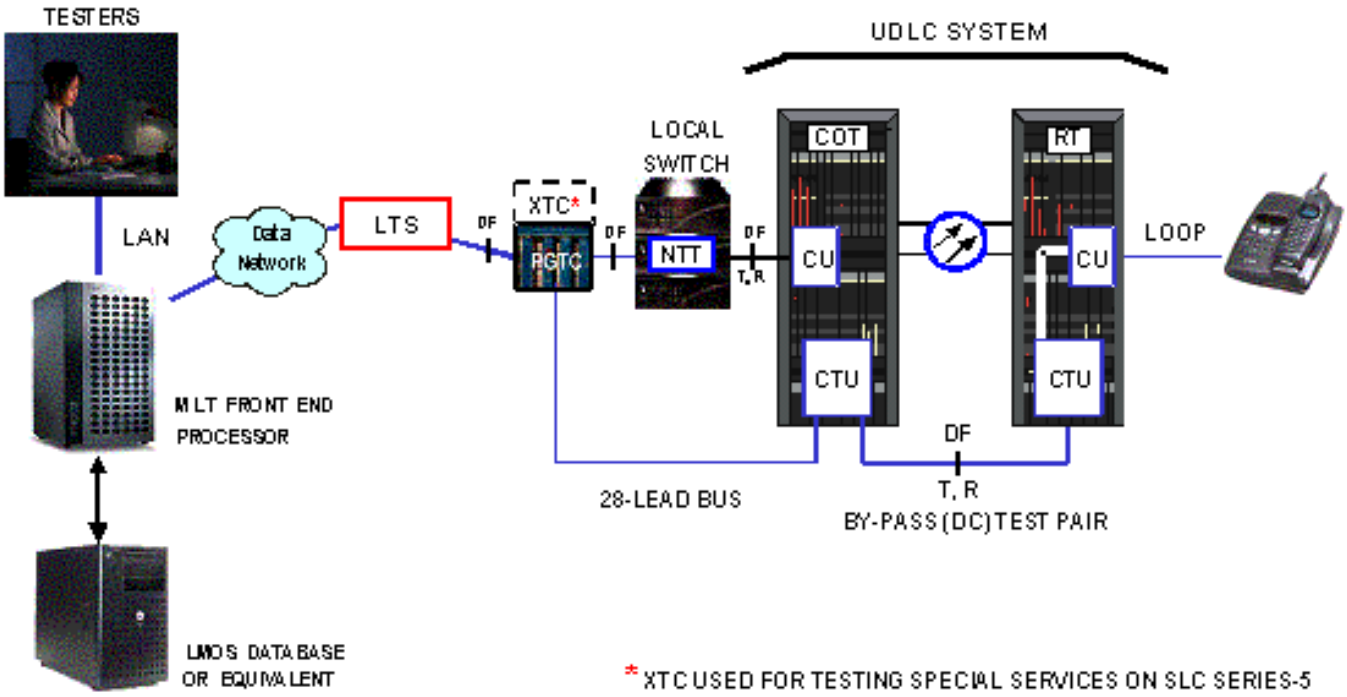


Figure 1•3 Universal DLC Testing

1.9. Integrated DLC Testing – 5ESS

Figure 1•4 is an example of Integrated DLC Testing for the 5ESS Switch.

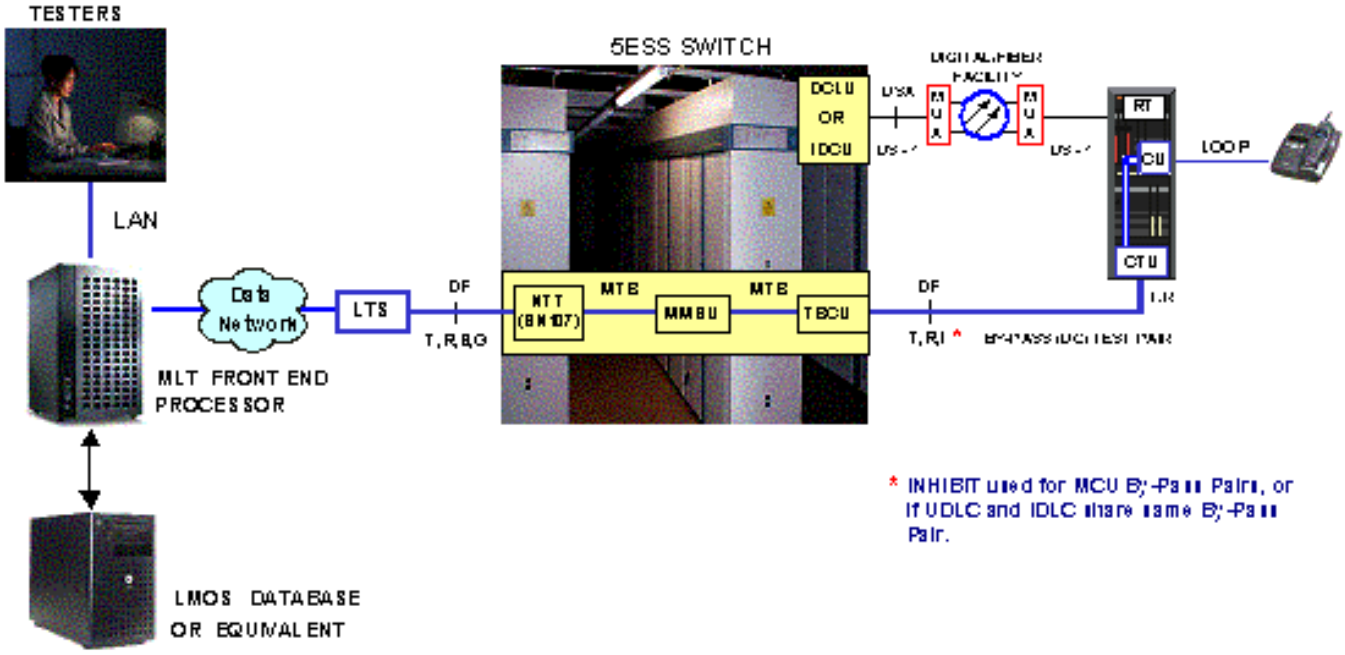


Figure 1•4 Integrated DLC Testing 5ESS

1.10. Integrated DLC Testing • 5ESS/IMLT (DCTU)

Figure 1•5 is an example of Integrated DLC Testing for the 5ESS/IMLT (DCTU) Switch.

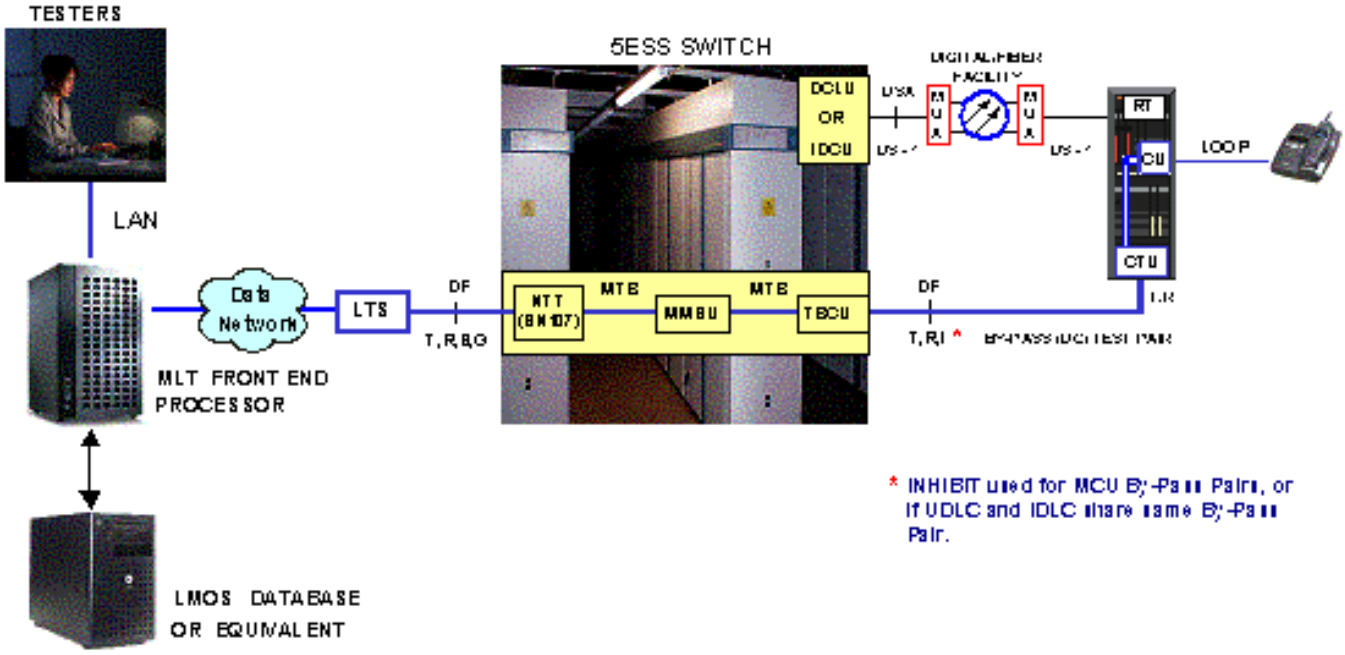


Figure 1•5 DLC 5ESS/IMLT (DCTU) Testing

1.11. Integrated DLC Testing – DMS—100

Figure 1•6 is an example of Integrated DLC testing for the DMS—100 Switch.

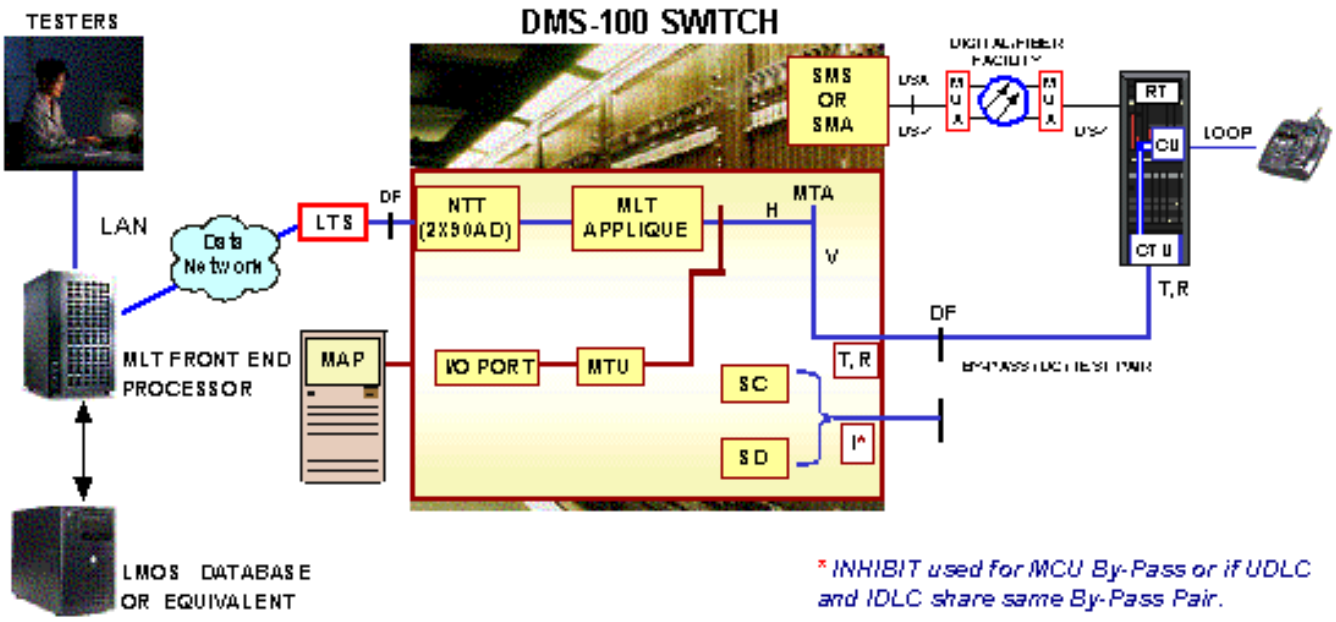


Figure 1•6 DLC DMS—100 Testing

1.12. Integrated DLC Testing – Siemen's (EWSD)

Figure 1•7 is an example of integrated DLC testing for the Siemen's EWSD.

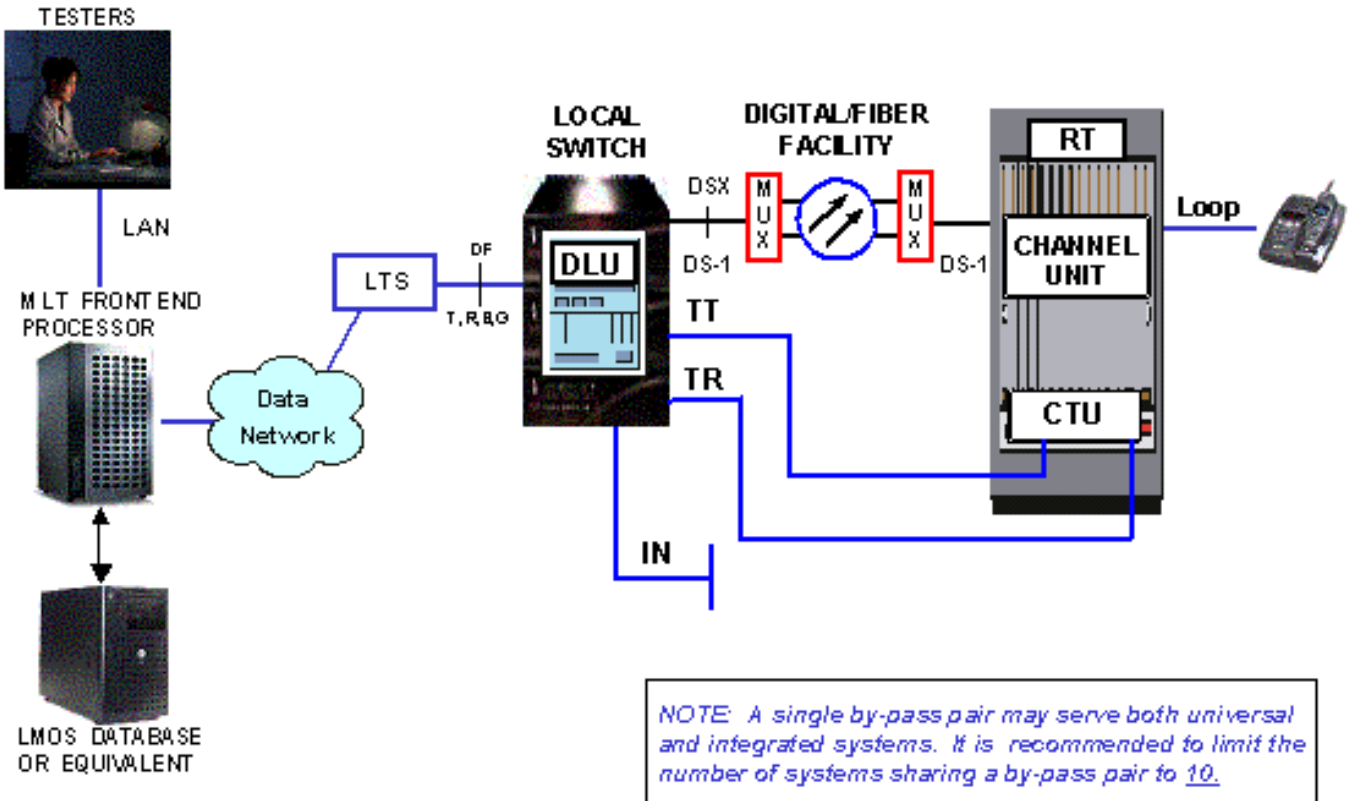


Figure 1•7 DLC EWSD Testing

1.13. MLT System Can Test

- Plain Old Telephone Service (**POTS**) Multiparty
- Coin
- Private Branch eXchange (**PBX**)
- Digital Loop Carrier (**DLC**)
- Integrated Services Digital Network (**ISDN**)
- Centrex
- Other circuits, such as alarm systems using MDF test shoe.

1.14. MLT – INDIVIDUAL TESTS AND MEASUREMENTS

- Hazardous Potential
- Busy Detection
- Foreign Electromotive Force (FEMF) Tests
- Electronic Speech Detection
- Line in Use Tests – confirmation of busy where no speech is present
- Receiver Off Hook Detection
- Intercept Detection
- Denies Service Detection
- Direct Current (DC) Tests – an array of configurable DC resistances and voltages
- PBX Identification
- Alternating Current (AC) Signature Identification (An array of configurable AC impedance and voltage)
- Longitudinal Balance Test
- Thermistor Test
- Open Detection and Measurement
- Line Circuit Test
- Draw and Break Dial Tone Test.
- Soak Test • Tests to measure variation in DC resistance over time, to determine if a ground is “swinging” and if it may be “dried out” by applying voltage.
- Ringer Test

- Length of Loop Measurement

1.15. Questions:

1. Name 3 methods to deliver dial tone.

2. Identify the 3 main test paths.

3. PGTC is used to test what?

SECTION 2 METALLIC, LTS, AND NTT TESTING

In This Section:

2.1 Lesson Overview

Loop Test System (**LTS**) is a microprocessor—based testhead that tests Plain Old Telephone Service (**POTS**).

It uses digital signal processing to calculate AC and DC equivalent signatures based upon three terminal measurements using 150v power amplifiers.

It is capable of detecting DC busy loops (with and without speech) by providing tracing tone and interactive tests.

No Test Trunks (NTT) reside in the switch and are the means to access subscriber lines.

2.2 Basic Metallic Loop Testing

Figure 1•2 is an example of test paths for POTS testing.

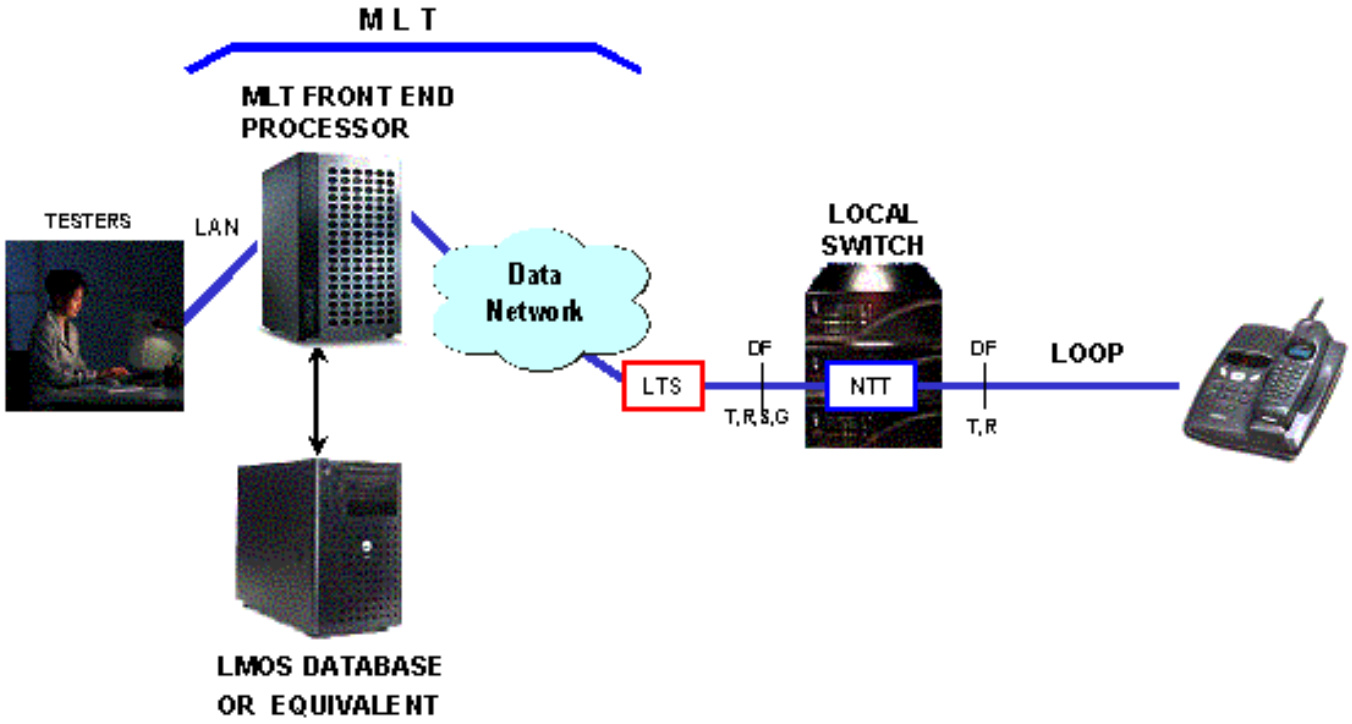


Figure 2•1 Basic Metallic Loop Testing

2.3 Fully Installed LTS Rack

Figure 2•2 is an example of a fully installed LTS rack.

Figure 2•2 Fully Installed LTS Rack

2.4 METALLIC, LTS, AND NTT TESTING ARCHITECTURE

Figure 2•3 is an example of the metallic, LTS, and NTT testing architecture.

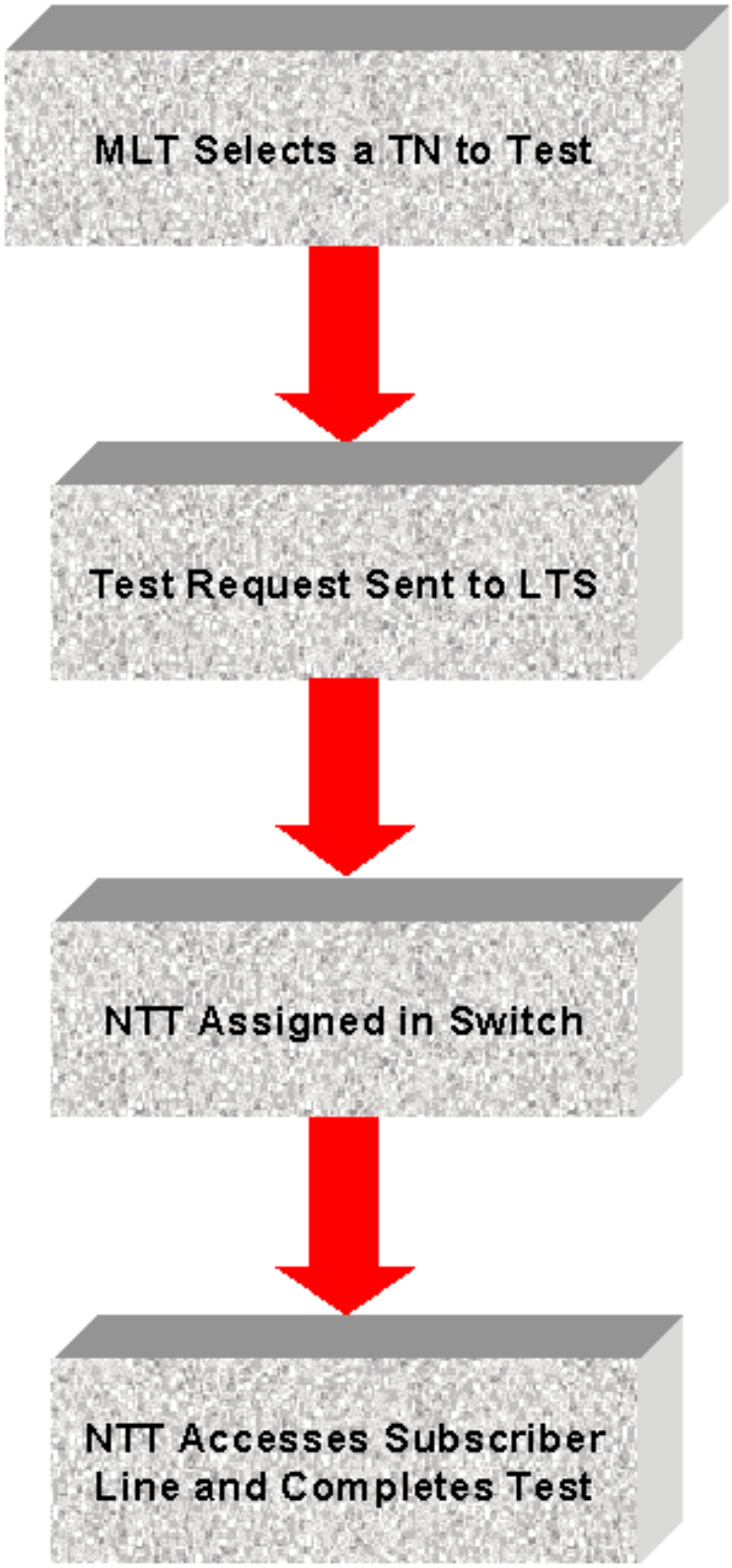


Figure 2•3 Metallic, LTS, and NTT Testing Architecture

SECTION 3 Universal DLC

Testing Applications Pair Gain Test Controller (PGTC)

In This Section:

3.1. Objectives

The student will be able to understand the operation and function of the PGTC, and be able to resolve MLT testing problems in the Universal Digital Loop Carrier architecture.

3.2. Universal DLC Testing Overview

Without some assistance, MLT cannot test Universal Digital Loop Carrier lines.

The main function of the Pair Gain Test Controller (PGTC) is to provide access to universal digital carrier lines so that MLT can test. ***PGTC has to be used***, because the Channel Units do not provide a metallic path between the COT and RT.

Figure 3•1 is an example of Universal DLC (UDLC) Testing:

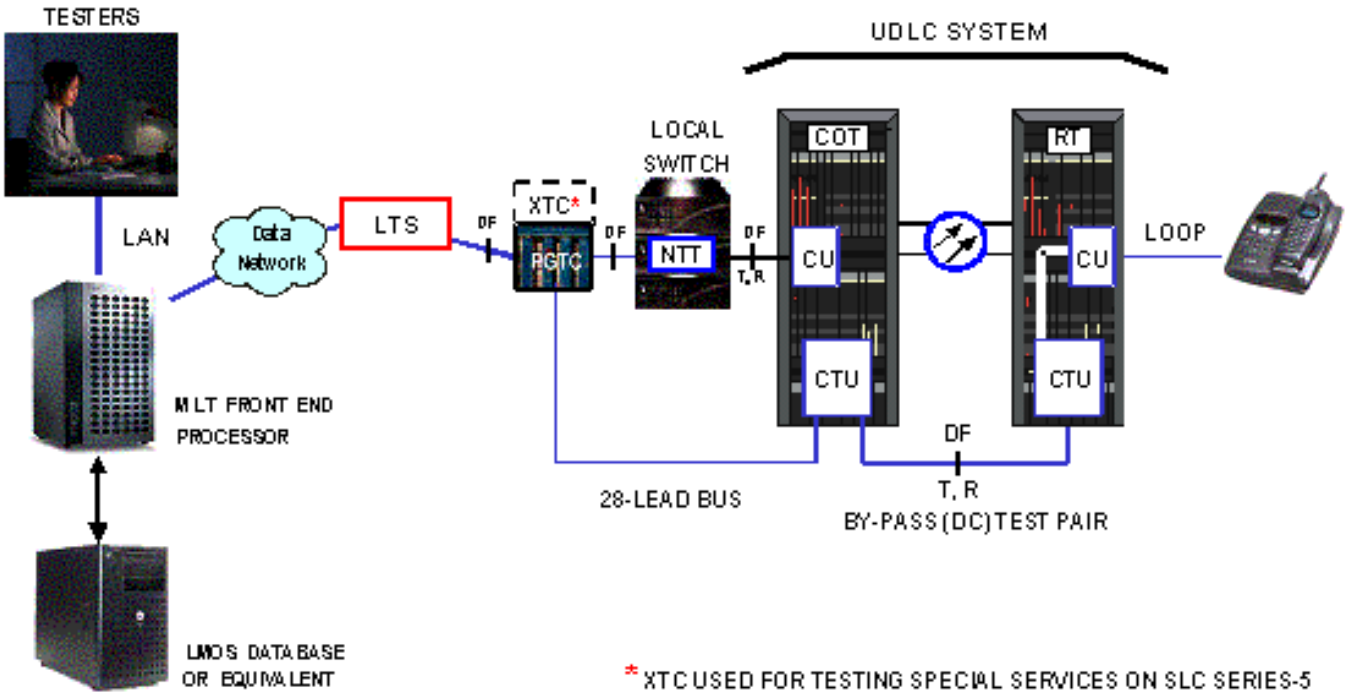


Figure 3•1 Universal DLC Testing using a PGTC

3.3. PAIR GAIN TEST CONTROLLER (PGTC)

The main test hardware in a Universal DLC environment:

- Provides metallic path by cutting-through metallic test pair (or emulated metallic test pair using Tollgrade MCU® units) from the CO to remote terminal (**RT**)
- Is a small unit mounted in office bay
- Is wired between test system LTS and No Test Trunks (**NTT**)
- Can assign NTTs to test copper, Universal or Integrated SLC.

Figure 3•2 is an example of a Universal DLC MLT Screen.

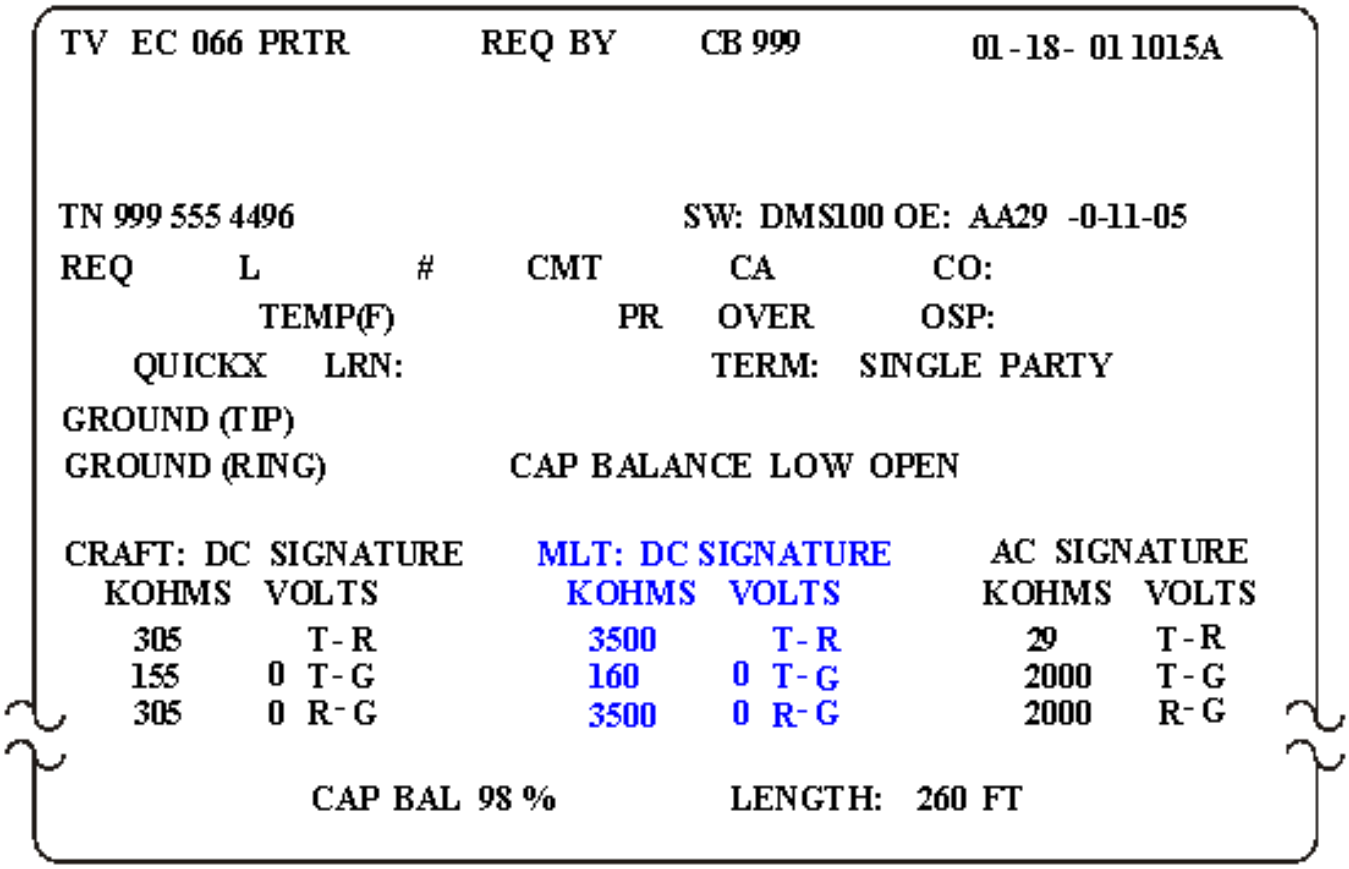


Figure 3•2 Universal DLC LoopCare Screen

To determine if you are testing Universal or Integrated SLC, run a "Quick Test". If Universal, you should see the following signature.

T – R 3500

T – G 165 Kohms

R – G 3500

NOTE: Universal DLC testing requires:

1. PGTC

2. NTT wired into PGTC

3. 28-pin daisy-chain through all Universal DLC systems within the CO

4. Working CTU * at CO

5. Working CTU at RT

6. Working CU ** at RT.

*** Channel Test Unit**

**** Channel Unit**

3.4. PGTC Control Shelf

- The control shelf is eight inches (8") high and is designed to fit into standard 23" framework.
- The control shelf requires –48 Vdc (signal grade) at 2.5 amperes (maximum) and uninterrupted ringing voltages wired to pin 10 of the PGTC at 0.5 amperes (maximum). Ringing should be 86 –100 Vac 20 Hz with superimposed –42.5 to –52.5 Vdc.

- Control shelf accommodates up to 12 No Test Trunks (NTT) – 2 trunks per 94C card.

3.5. PGTC CONTROL SHELF

Figure 3•3 is an example of PGTC Control Shelf.

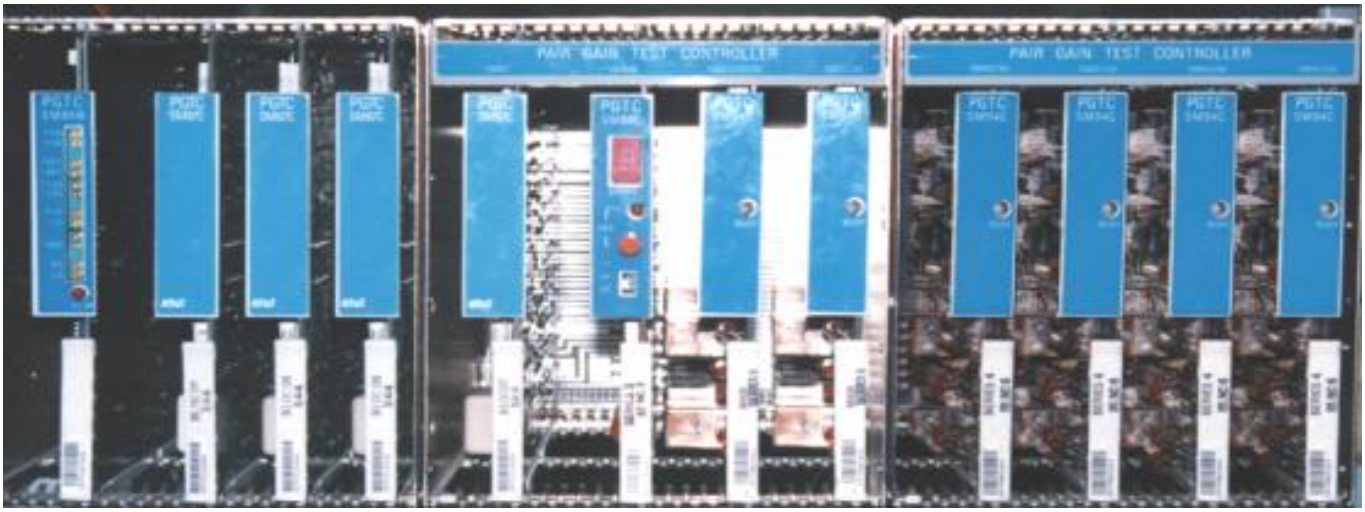


Figure 3•3 PGTC Control Shelf

3.6. PGTC CONTROL SHELF

Figure 3•4 is an example of PGTC Control Shelf.

86	TESTER UNIT				88	NO TEST TRUNKS					
POWER	A	B	C	D	CONTROL	1	3	5	7	9	11
	87C	87C	87C	87C		94C	94C	94C	94C	94C	94C
						2	4	6	8	10	12

Figure 3•4 PGTC Control Shelf Diagram

3.7. SEQUENCE

When a PGTC needs to run a test, it picks Tester **"A"** first **EVERY TIME**.

- If "**A**" is busy, it goes to Tester "**B**".

If "**A**" and "**B**" are busy, it goes to Tester "**C**".

- If "**A**" and "**B**" and "**C**" are busy, it goes to Tester "**D**".

NOTE: The maximum number of Universal DLC tests that can be run in any office at one time is four (4).

3.8. PGTC Functionality

NOTE: The following conditions will exist if access line is idle, and LMOS lists subscriber as being on DLC system.

1. +116v placed on Tip side of line to wake up DLC channel unit.
2. Not seen as a coin disposal potential since ringside isn't grounded.
3. Channel unit activates PGTC and orders Channel Test Units (**CTUs**) to cut to Metallic Test Path (**MTP**) through drop.
4. After cut-through, screener can perform detailed loop tests:
   - Metallic testing
   - Ringer count
   - Application of trace tone.

- If MLT sees a valid DLC signature upon access, it will initiate Pair Gain Testing Access (with or without live records).
- The MTP can be shared by up to **10** banks on the same RT site. Banks have Tip (**T**), Ring (**R**), and Inhibit (**I**) leads multiplied at the block on the same Distributing Frame (**DF**).
- T and R are also multiplied at the RT banks.
- T and R are the actual MTP and the 'I' lead prohibits access by more than one CTU at a time.
- All SLC 96 and Feature Package A (**FPA**) and FPB Series-5 SLC COT bank CTUs are tied to the PGTC with a 28-lead "*daisy-chain*" control bus located at the top of the COT bays.
- The PGTC can access any CTU and associated MTP.
- The PGTC also performs an auto test of the T1 channel from the COT to the RT. Results are sent to the tester and can be seen in a display window in the PGTC.
- Tests include:
  - Good signal party channel
  - Good multi-party channel
  - Good coin channel
  - Bad carrier channel.

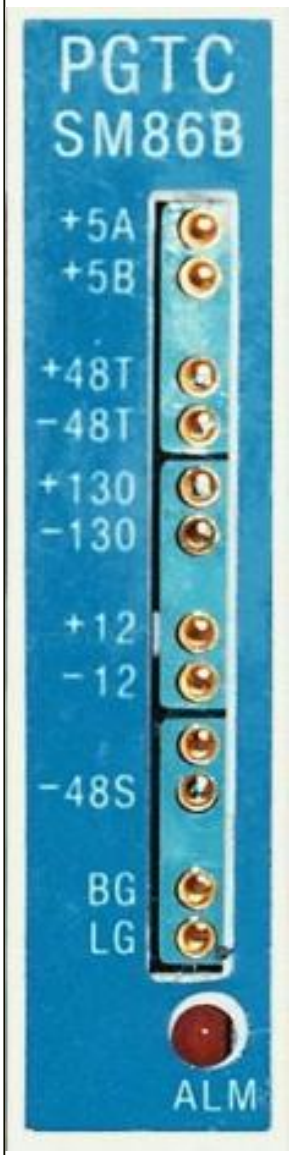
NOTE: With a 5ESS switch, all plug-ins must meet specific vintage requirements (as represented in the following sections)..

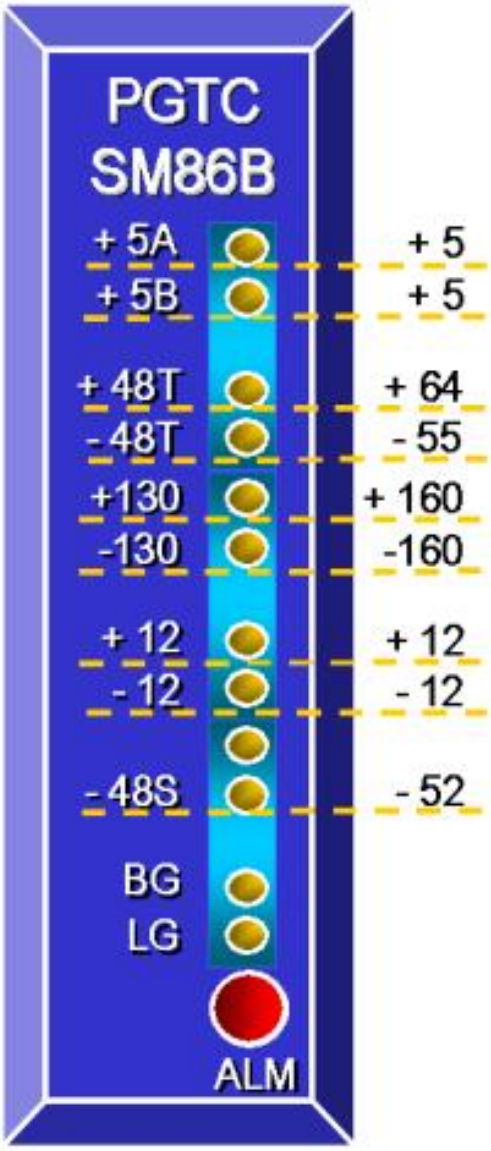
3.9. PGTC CIRCUIT PACKS

3.9.1. SM86 POWER PACK

Slot 1 of the control shelf contains an SM86 Power Unit. This required circuit pack provides power for the other circuit packs and control signals within the control shelf. Test jacks are provided on the face of the SM86 for the measurement of input and output voltages Figure 3•5 page 3•9 shows the measurement requirements for turning up the control shelf. An alarm lamp is also located on the front to indicate trouble within the PGTC.

Figure 3•5 and diagram shows examples of the PGTC SM86 Power Pack.





- **The first slot contains an SM86 circuit pack, providing power for the other packs and control signal within the shelf.**
- **The SM86 requires a •48 Vdc signal grade input to generate outputs of +5, +12, +48, •48, +130 and •130 Vdc. The •48 Vdc is a filtered talk-grade battery supply.**
- **Test jacks are provided on the face of the pack for measurement of input and output voltages.**

Figure 3•5 SM86 Power Pack

NOTE: SM86 boards should have a current "B" Alpha Designation.

3.9.2. SM87 TESTER UNITS

Figure 3•6 is an example of PGTC SM87 Tester Unit.

- **Slots 2, 3, 4 and 5 contain the SM87 Tester Units which are referred to as the A, B, C, and D Tester Units.** ***(See Figure 3•3 on page 3•5, and Figure 3•4 on page 3•6)***

- **Each Unit provides the circuitry necessary for performing the automatic testing of the channel.**

- **Initial testing will attempt to select Tester A. If that unit is busy, the test request proceeds to Tester B, etc.**

Figure 3•6 SM87 Tester Units

NOTE: SM87 boards should have a current "C" Alpha Designation, series 3 or later.

3.9.3. SM88 Control Units

Figure 3•7 is an example of PGTC SM88 Control Units.

- **Slot 6 contains the SM88 Control Unit, which provides the common control circuitry for the PGTC.** ***(See Figure 3•3 on page 3•5, and Figure 3•4 on page 3•6)***

- **The common control circuitry is in the form of a micro-controller package and associated interface circuitry.**

- **Within the micro-controller is a program that directs the operation of the control unit.**

Figure 3•7 SM88 Control Units

NOTE: SM88 boards should have a current "D" or "C" Alpha Designation. SM88 boards should utilize Series 3 or later in "C" cards.

3.9.4. SM94C TRUNK UNITS

Figure 3•8 is an example of **PGTC SM94C** Trunk Units**.**

- **Installed into slots 7 through 12, the SM94C Trunk Units provide a means of connecting any two test trunks to any of the available four tester units. This set-up is referred to as random access.** ***(See Figure 3•3 on page 3•5, and Figure 3•4 on page 3•6)***

- **The Control Unit allows the Trunk Units to interact with an available Tester Unit to permit the NO TEST TRUNK to be switched from the switching system to the subscriber's loop.**

Figure 3•8 SM 94C Trunk Units

NOTE: SM94 boards should have a current "C" Alpha Designation. SM94 boards should utilize Series 4 or later in "C" cards.

3.10. PGTC EXPANSION SHELF

When there is a requirement to wire more than 12 NTTs to the PGTC, an expansion shelf is needed. (The following graphic shows the Expansion Shelf configuration)

- The Expansion Shelf unit is connected to the control shelf and has its own power supply
- The Expansion Shelf must be physically located just below the Control Shelf
- The Expansion Shelf has its own power supply and supports up to 20 additional trunks (2 trunks per 94C card)
- A maximum of 4 Expansion Shelfs may be installed.

Figure 3•9 is an example of PGTC Expansion Shelf.

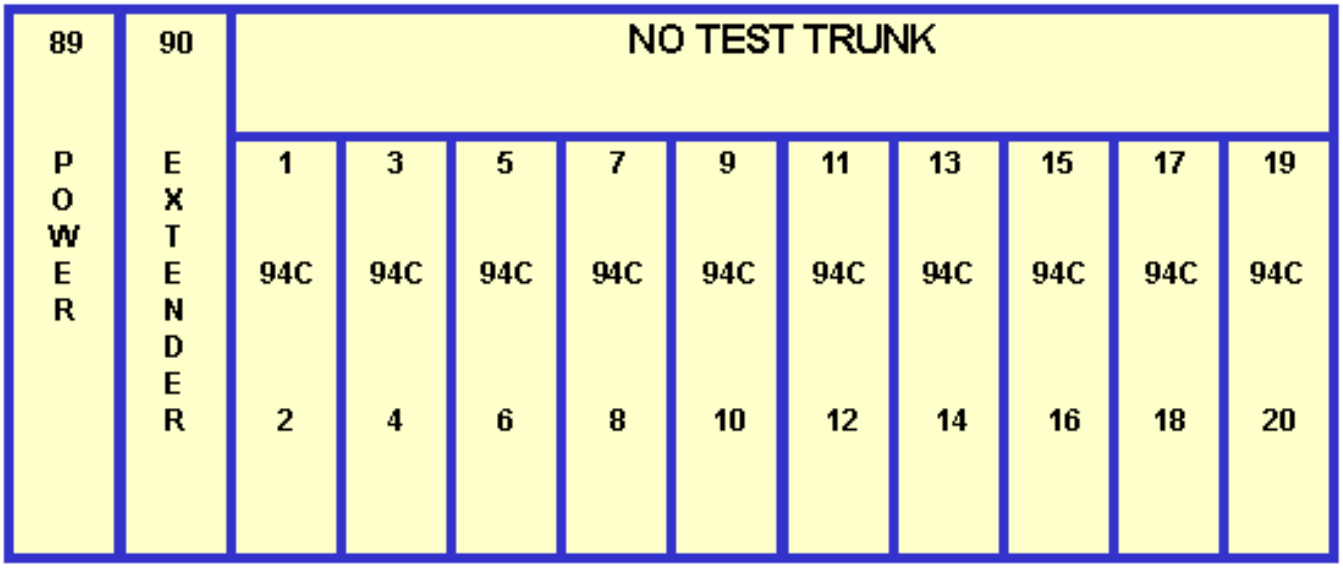


Figure 3•9 PGTC Expansion Shelf

3.11. Exercise: Technical Operation of the PGTC

Figure 3•10 is an example of PGTC Technical Operation**:**

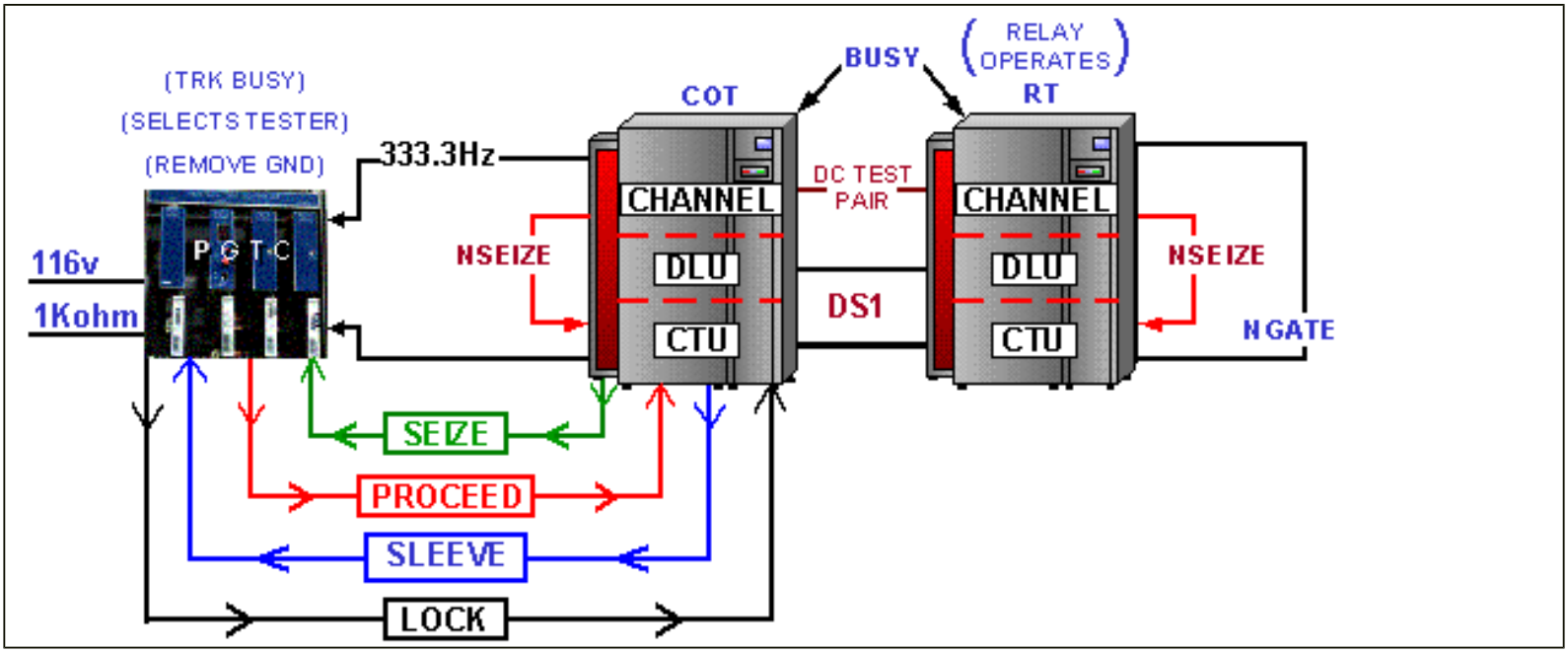


Figure 3•10 PGTC Technical Operation

The technical operation of the PGTC is described in the following steps:

Table 1 Technical Operation of the PGTC

STEP	DESCRIPTION
1.	When +116 Vdc or a minimum of +87 Vdc is applied from MLT to the Tip side of the circuit, the COT channel unit applies a 333.3Hz tone to the T and R leads back to the PGTC.
2.	At the PGTC, a tone detector in the SM94 Trunk Unit detects the tone and presents information to the SM88 Control Unit. Additionally, a GREEN busy lamp will light on the SM94 Trunk Unit.

3.	An NSeize command is output from the COT channel unit to the COT CTU and over the digital line to the RT channel unit.
4.	An NSeize command is output from the RT channel unit to the RT CTU and over the digital line to the COT channel unit.
5.	The COT CTU outputs a Seize command to the PGTC SM88 Control Unit.
6.	The SM88 Control Unit selects an available A through D Tester Unit and runs internal tests.
7.	The PGTC sends a PROCEED command to the COT CTU which is transmitted to the RT CTU via the DLUs.
8.	The RT CTU will issue an NGATE command to all RT channel units.
9.	The channel unit at the RT that previously received the NSeize command will connect its Tip and Ring to the CTU by operating a relay within the channel unit.
10.	A busy lamp lights on the COT and RT channel units.
11.	The COT CTU outputs a SLEEVE command to the SM88 Control Unit.
12.	The SM88 Control Unit outputs a LOCK command to the CTU.
13.	The SM88 Control Unit removes the ground placed earlier during the PROCEED step.

14.	The PGTC places a 1KOhm resistance on the Tip lead towards MLT to indicate that a test connection is established.

At this point, the MLT test will be completed normally. A by-pass of the electronics is effectively completed.

3.12. PGTC No Test Trunk Wiring

Figure 3•11 is an example of PGTC No Test Trunk Wiring.

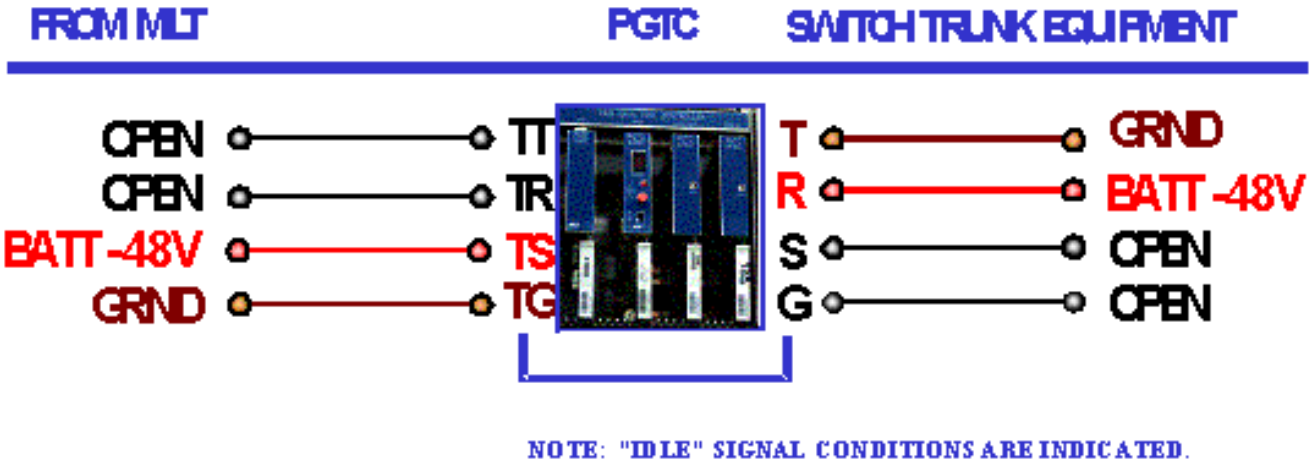


Figure 3•11 PGTC No Test Trunk Wiring

3.13. PGTC LEAD WIRING TO SLC SYSTEMS

- From the **PGTC** to each system, a continuous **25** pair cable, containing the **28-leads**, is chained through **Amphenol** plugs to each **SLC** system. Each of the 4 **PGTC** Tester Units (**A, B, C, D**) have:
  - **6** leads from the **PGTC** unit to the **SLC** systems.

– **T**ip	– **O**H	– **L**OK

– **R**ing	– **P**ROC	– **S**LV

4 common leads connecting the **PGTC** to the **SLC** systems.

– **ALM** (or **TSTALM**)	– **SEIZE**
– **TMAJ**	– **SEIZE-BY**

3.14. PGTC LEAD WIRING TO DLC SYSTEMS

Table 2 PGTC Lead Wiring to DLC Systems

PGTC Term	36	41	32	42	31	40	28	35	29	34	39	27				
Lead	**PROC-A**	**PROC-B**	**PROC-C**	**PROC-D**	**LOK-A**	**LOK-B**	**LOK-C**	**LOK-D**	**ALM**	**TMAJ**	**SEIZE**	**SEIZE BY**				
LS - 2000 J13/J14	34	9	35	10	36	11	37	12	42	17	47	22				
DISC*S	34	9	35	10	36	11	37	12	42	17	47	22				
FUJITSU FDLC CN6/CN7	34	9	35	10	36	11	37	12	42	17	47	22				
Series -5 CTU Term	63	64	65	66	67	68	69	70	71	78	72	73				
SLC-96 CTU Term	13	14	15	16	19	22	21	20	18	27	53	54				
SLC - 2000	34	9	35	10	36	11	37	12	42	17	47	22				
V/Ohm Result	-48V	-48V	-48V	-48V	-48V	-48V	-48V	-48V	-48V	-48V	-48V	-48V				
PGTC Term	14	15	17	18	20	21	23	24	26	37	30	38	16	19	22	25
Lead	**T-A**	**R-A**	**T-B**	**R-B**	**T-C**	**R-C**	**T-D**	**R-D**	**SLV-A**	**SLV-B**	**SLV-C**	**SLV-D**	**OH-A**	**OH-B**	**OH-C**	**OH-D**
LS - 2000 J13/J14	26	1	27	2	28	3	29	4	30	5	31	6	32	7	33	8

LS - 2000 J13/J14	26	1	27	2	28	3	29	4	30	5	31	6	32	7	33	8
DISC*S	26	1	27	2	28	3	29	4	30	5	31	6	32	7	33	8
FUJITSU FDLC CN6/ CN7	26	1	27	2	28	3	29	4	30	5	31	6	32	7	33	8
Series 5 CTU Term	58	57	56	55	54	53	52	51	74	75	76	77	59	60	61	62
SLC-96 CTU Term	37	36	34	33	30	29	32	31	51	52	4	1	5	7	10	9
SLC - 2000	26	1	27	2	28	3	29	4	30	5	31	6	32	7	33	8
V/Ohm Result	CAP.	CAP.	CAP.	CAP.	CAP.	CAP.	CAP.	CAP.	-48 V	-48 V	-48 V	-48 V	-48 V	-48 V	-48 V	-48 V

3.15. PGTC 28-LEAD DAISY-CHAIN CONTROL BUS

Figure 3•12 is an example of the **PGTC 28•Lead** daisy•chain control bus.

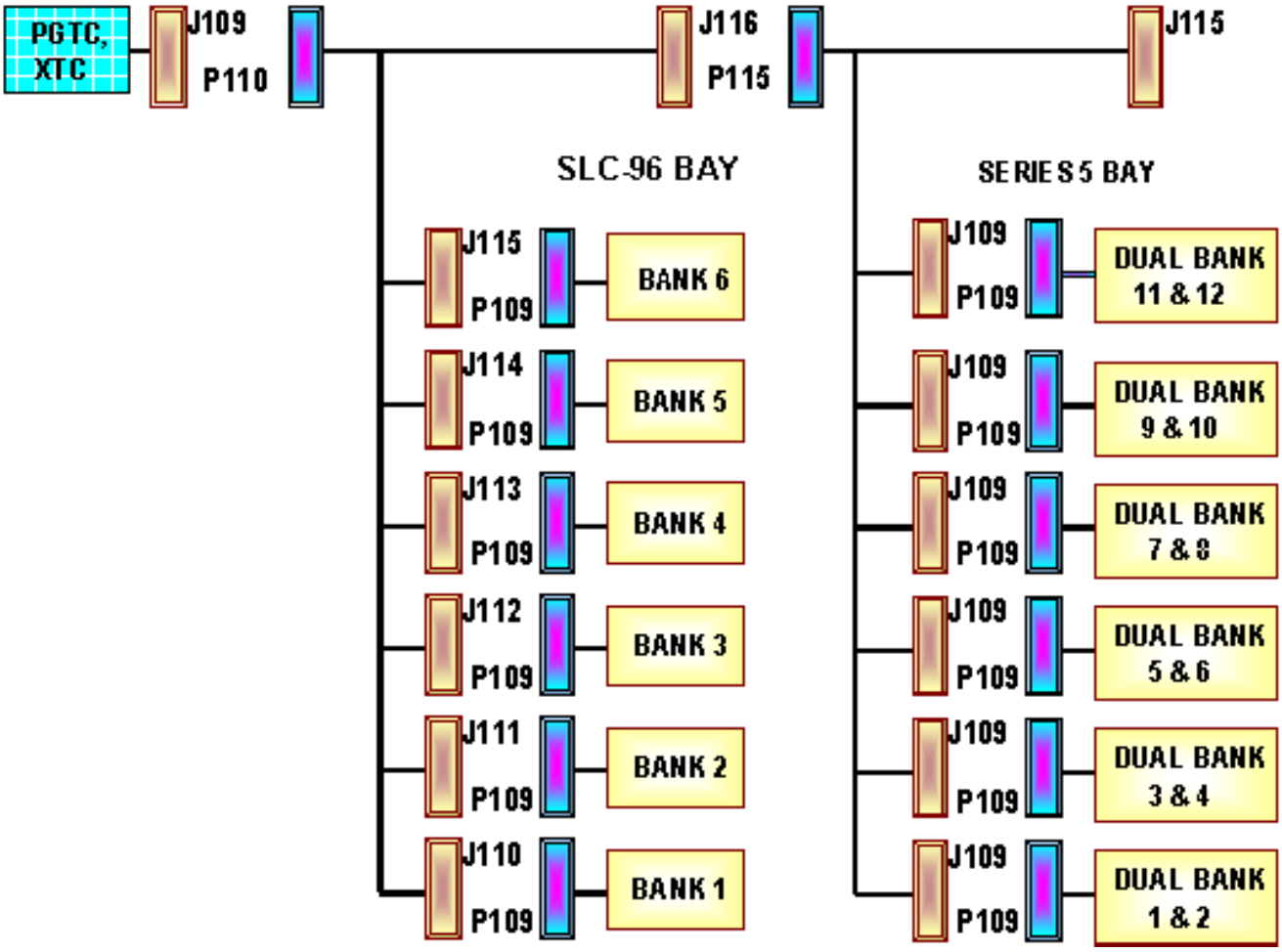


Figure 3•12 PGTC 28-Lead Daisy-Chain Control Bus

3.16. TRADITIONAL DLC TESTING – METALLIC BY-PASS PAIR

Description: Copper DC Test Pair Architecture.

Figure 3•13 represents the Traditional **DLC** Testing • Metallic By•Pass Pair architecture.

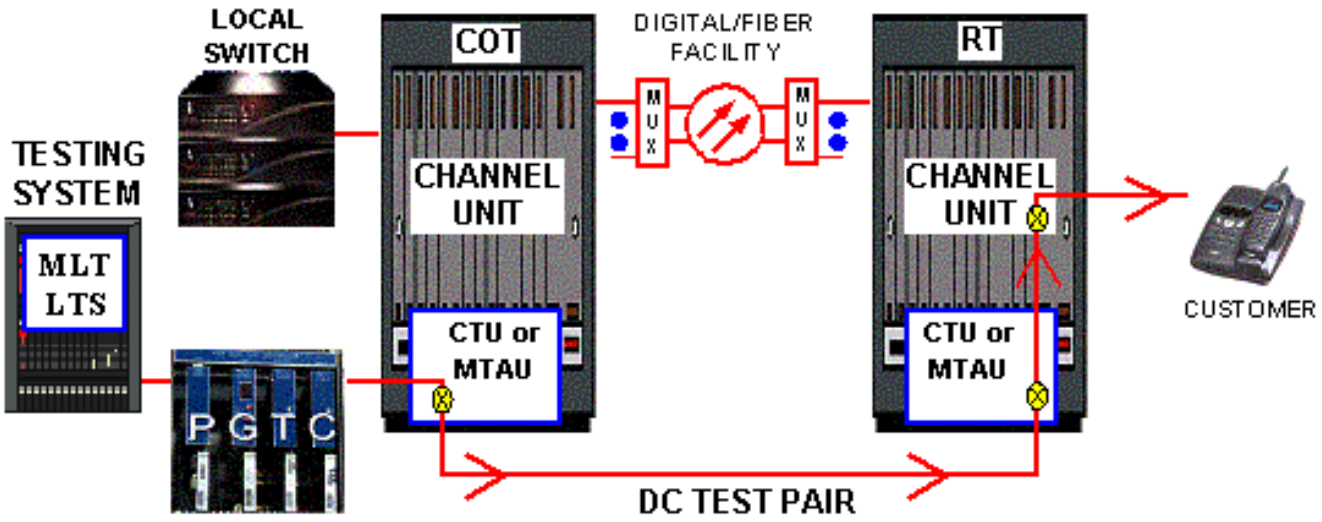


Figure 3•13 Traditional DLC Testing - Metallic By-Pass Pair

3.17. TOLLGRADE METHOD – DIGITAL BY-PASS PAIR

Description: MCU Technology Architecture.

Figure 3•14 represents the MCU technology architecture.

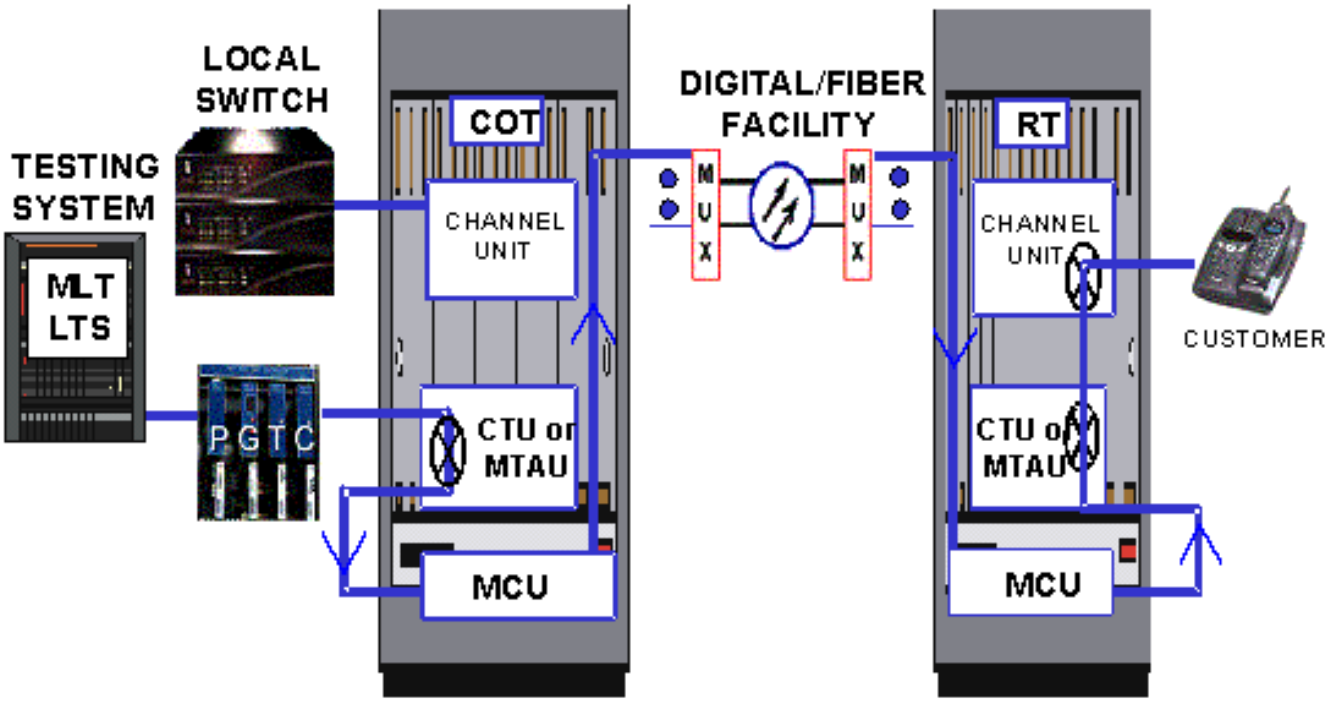


Figure 3•14 Tollgrade Method - Digital By-Pass Pair

3.18. TIP RING and INHIBIT ORIGINATION POINT

Table 3 is an example of the Tip, Ring, and Inhibit Origination Point architecture.

Table 3 Tip, Ring, and Inhibit Origination Point.

	SLC 96 CTU PIN OUT	SLC SERIES 5 CTU PIN OUT		FUJITSU FDLC	DSC LITESPAN-2000
		A BLUE	B WHITE	TRM 1	TB8 JI

SLC 96 RT – Wiring for DC test pair – Provides the metallic path from the CO to-and-through the remote tunnel. DC test pair for MCU tip and ring is wired to the J107 Pair 5 and then internally to the SLC 96 Systems 1, 2, 3, etc. (For further information see PTAP Reference Documents Section 2 **Error! Reference source not found.** page **Error! Bookmark not defined.**.)

Figure 3•15 is an example of the SLC 96 RT – Wiring for DC test pair.

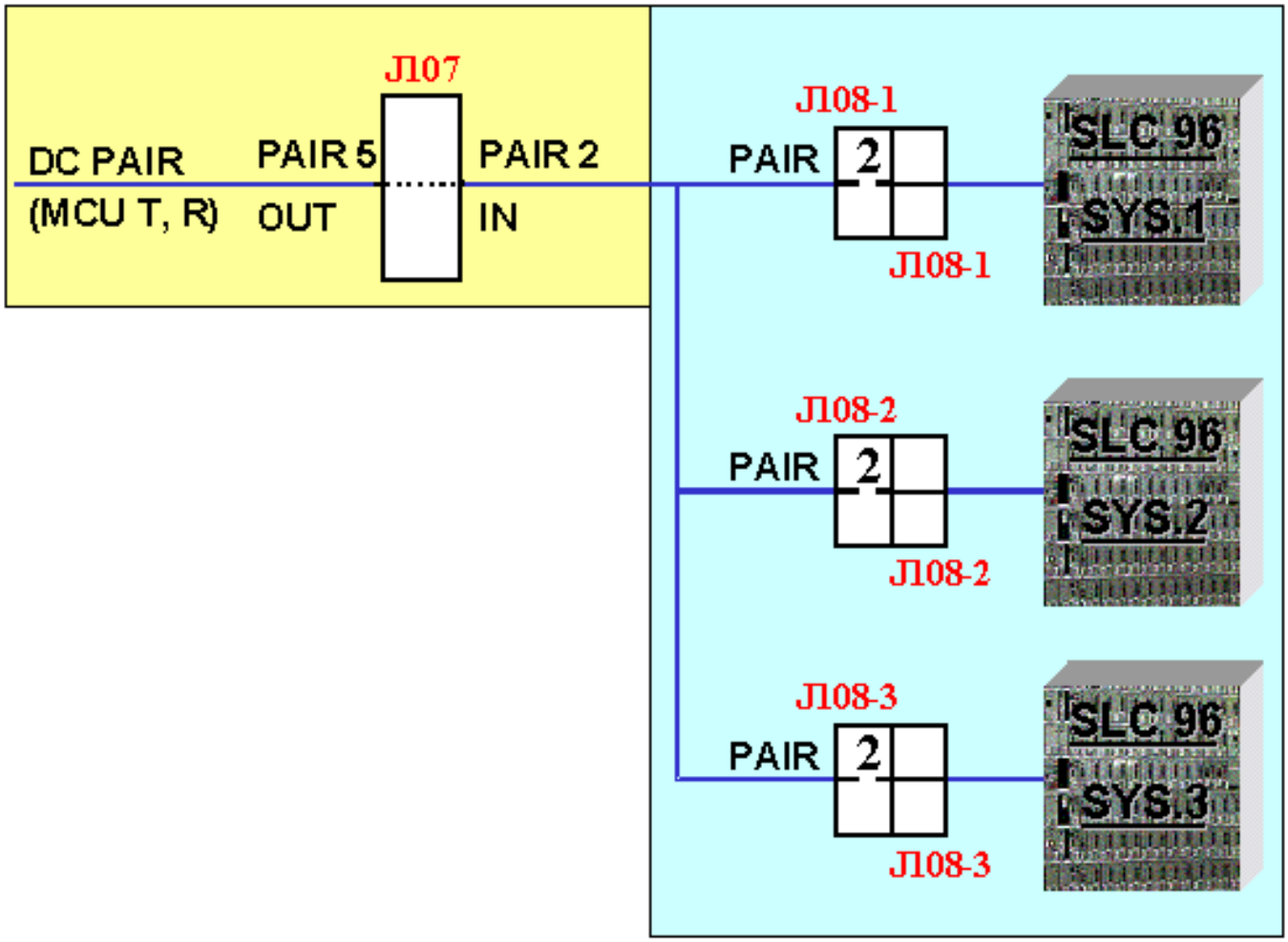


Figure 3•15 SLC 96 RT – Wiring for DC Test Pair

T = Tip

R = Ring

I = *INHIBIT*

Voltage Measured to Ground

ATTENTION!

When CTUs/MCUs are idle, you will see:

At the Central Office:
T = 0
R = -48V
I = -48V
At the RT:
T = 0
R = -48V

When CTUs/MCUs are busy, you will see:

At the Central Office:
T = 0
R = 0
I = GND
At the RT:
T = 0
R = 0

NOTE: Inhibit lead wiring is necessary because another test could come in over top. You need to remove battery from R. If you don't, you will see a cross to a working pair (referred to as a false test).

1.16. QUESTIONS

1. What is the main function of the PGTC?

SECTION 4 Integrated DLC Testing Applications

In This Section:

4.1. Objectives

The student will understand the MLT testing paths for integrated digital loop carrier testing.

4.2. Lesson Overview

This lesson will introduce the most important Integrated DLC Testing Application, and how they are utilized.

The following are examples of the Integrated DLC Testing Applications:

- 5ESS – TBCU
- DMS-100 – IDLC TESTING

- Siemens' (EWSD) DLU.

4.3. INTEGRATED DLC TESTING - 5ESS TBCU overview

- For Integrated DLC testing in a 5ESS, the Test Bus Control Unit (TBCU) performs the IDLC test function.
  - If a 5ESS is equipped with both Universal and Integrated DLC, **both** the PGTC and the TBCU are required.
  - The TBCU replaces the PGTC **only** with IDLC.

Figure 4•1 is an example of the Integrated DLC Testing - 5ESS.

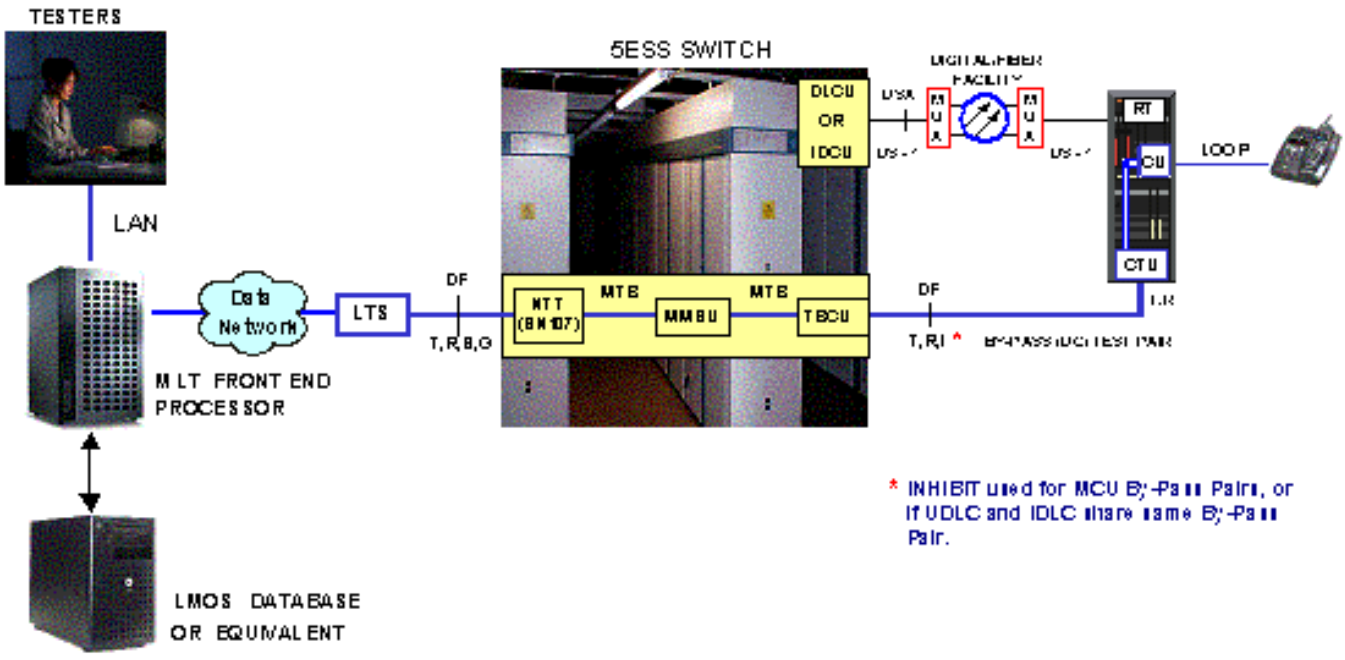


Figure 4•1 Integrated DLC Testing - 5ESS

4.4. DMS-100 – IDLC Testing Overview

- The DMS Switch also has IDLC capability.
- It uses a Metallic Test Access (MTA) circuit (similar to the MSU), Subscriber Multiplexer SLC 96 (SMS) interfaces (similar to DCLUs or IDCUs), and Pair Gain Applique (similar to the TBCU).

Figure 4•2 is an example of the DMS-100 – IDLC Testing Architecture.

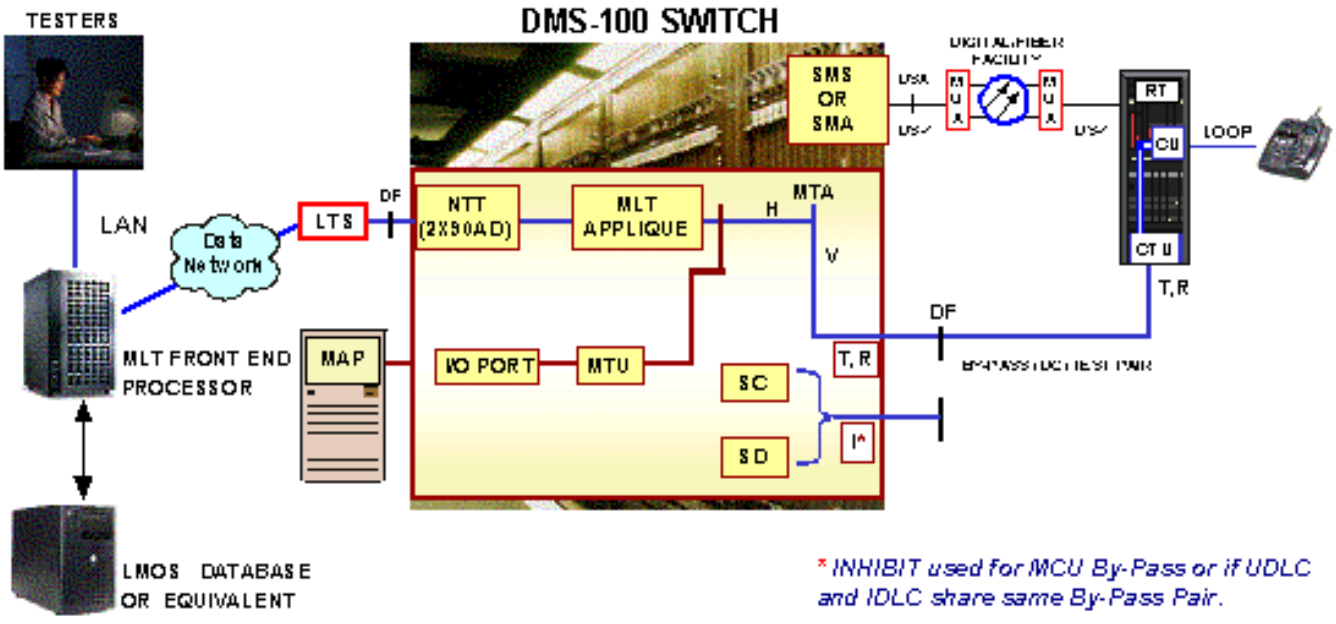


Figure 4•2 DMS-100 – IDLC Testing Architecture

4.5. DMS-100 – UDLC/IDLC Testing Architecture

Figure 4•3 is an example of the DMS-100 – UDLC and IDLC Testing Architecture.

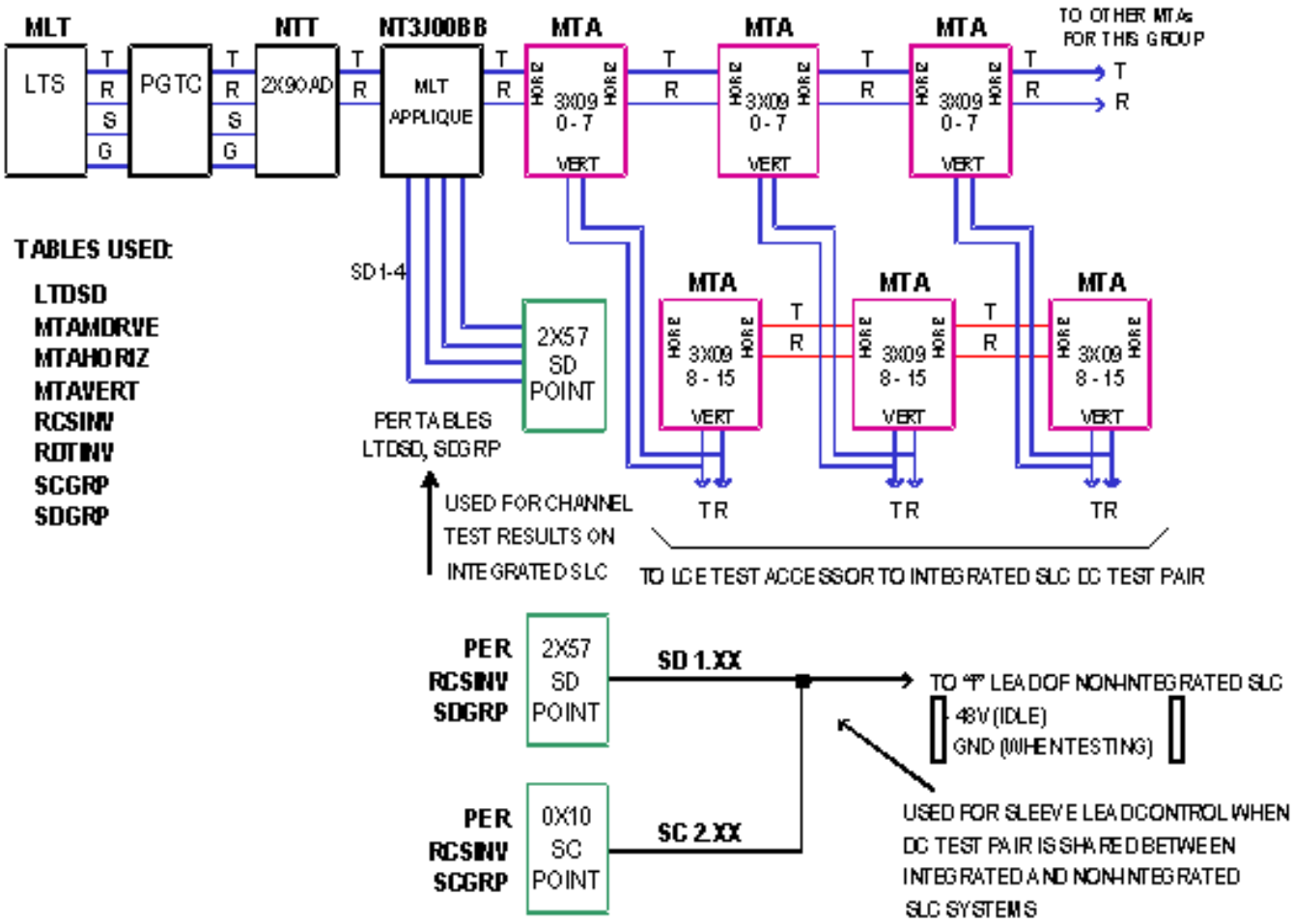


Figure 4•3 DMS-100 – UDLC and IDLC Testing Architecture

4.6. Siemen's (EWSD) Testing Overview

- Most Tollgrade customers configure the Alcatel Litespan System for both Universal and Integrated service, plus multiple Remote Terminal (RT) configurations, East and West.
- The Universal system will use test pair #1, while the integrated systems may use either test pair #1 or test pair #2, depending on the Interface Group software setting.
- The EWSD switch architecture provides for a limit of 18 integrated systems (DLUs) that may share a Metallic Test Path (Tollgrade MCU®-D405).

Therefore, a challenge exists when connecting to an Alcatel Litespan DLC with multiple RTs.

Figure 4•4 is an example of DLC Testing for the Siemen's (EWSD).

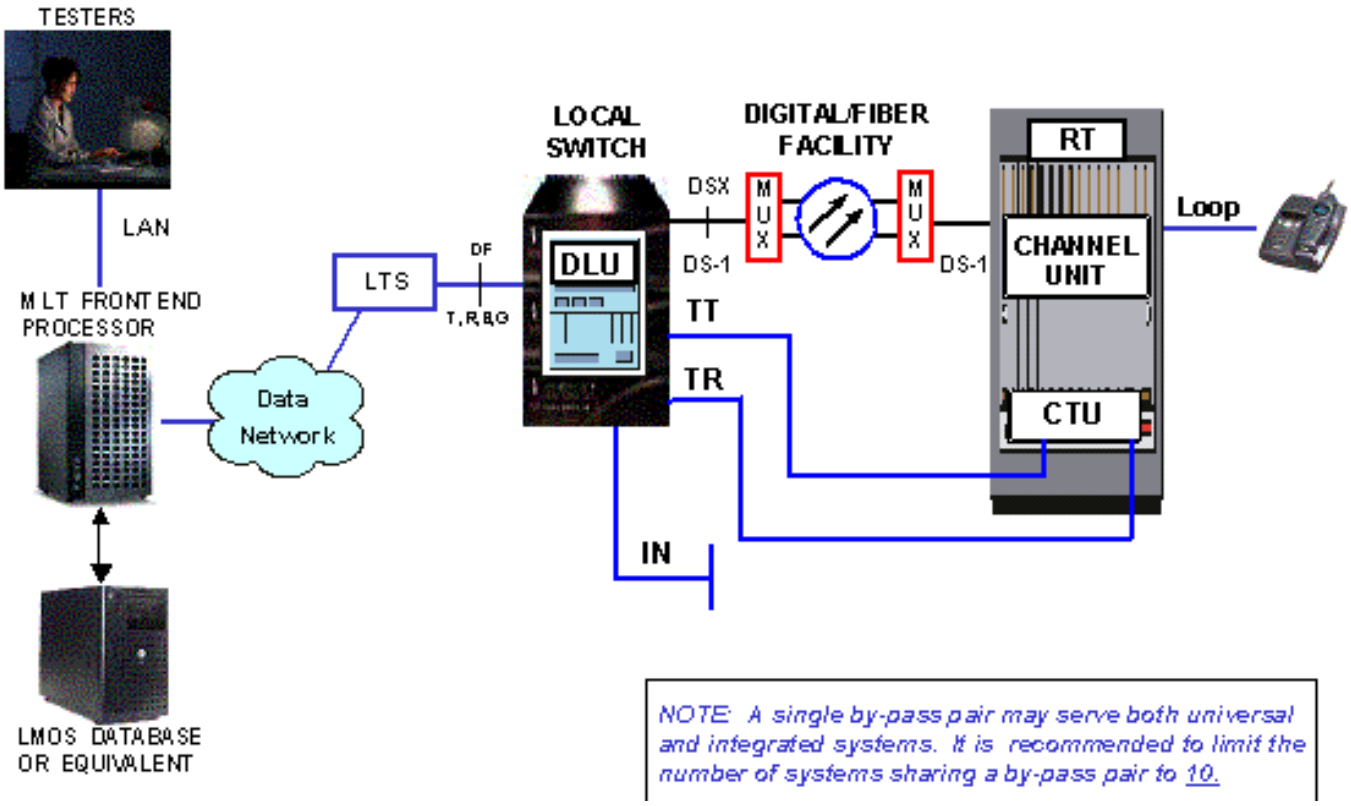


Figure 4•4 DLC EWSD Testing

4.7. Quick Test of an Integrated DLC Line

Figure 4•5 is an example of a Quick Test of an Integrated DLC Line.

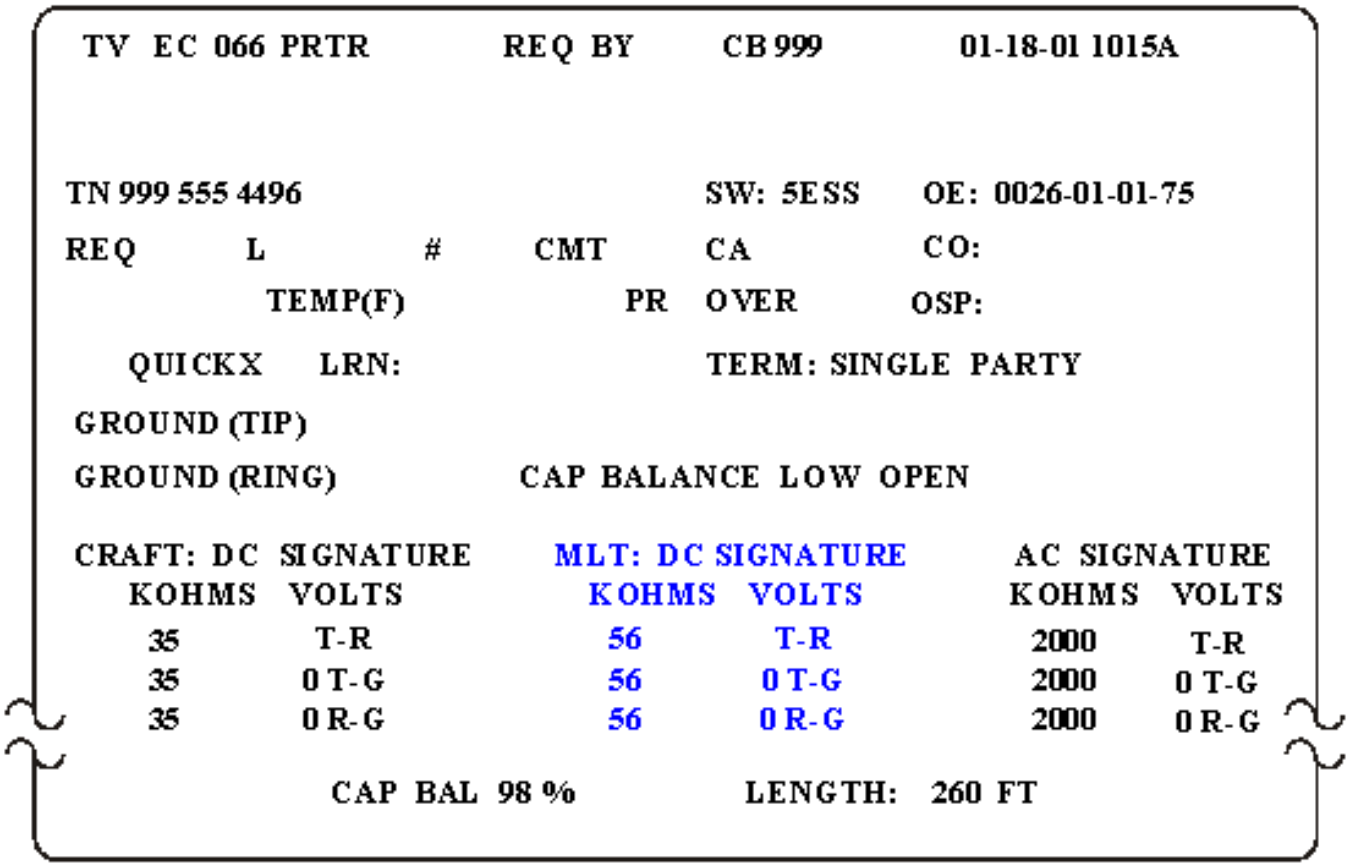


Figure 4•5 Quick Test of an Integrated DLC Line

4.8. questions

1. What is the electronic signature of an integrated digital loop carrier line?

2. Is the PGTC required for testing integrated digital loop carrier lines?

SECTION 5 Integrated DLC Testing - Lucent 5ESS Switches

In This Section:

5.1. objectives

The student will understand the hardware and software required for IDLC testing in a 5ESS switch.

5.2. 5ESS LOOPCARE/mlt TESTING ISSUES COURSE OVERVIEW

- LoopCare/MLT Overview
- Integrated LoopCare Overview
  - Integrated MLT Datalink

- Directly Connected Test Unit (DCTU)
- Modular Metallic Service Unit (MMSU)
- Test Bus Control Unit (TBCU)
- Pair Gain Test Controller (PGTC)

5.3. LOOPCARE/MLT SYSTEM OVERVIEW

- Automated Test System.
- Performs on-demand or pro-active (Program scan, ALIT).
- Analyzes problems on CO, Outside Plant and Customer Premise Equipment (CPE).
- Can perform rapid and interactive tests.
- Provides **VER Codes** to permit automated screening.

5.4. LOOPCARE/MLT ARCHITECTURE

- Application software - resides in transaction processor
- Operating system/Database (LMOS)
- LAN - Connects testers to processor
- DCN - Connects processor to test hardware
- Test hardware:

- LTS - Loop Test System
- DCTU - Directly Connected Test Unit (5ESS)
- PGTC - Access to Universal DLC
- TBCU - Access to Integrated DLC (5ESS)

5.5. LOOPCARE/MLT SYSTEM TESTS

- Plain Old Telephone Service (POTS)
- Multiparty
- Coin
- Private Branch Exchange (PBX)
- Digital Loop Carrier (DLC)
- Integrated Services Digital Network (ISDN)
- Centrex
- ADSL
- Other circuits, such as alarm systems using test “shoe”

5.6. LOOPCARE/MLT TESTS/MEASUREMENTS

- Hazard potential
- Busy detection
- Foreign Electromotive Force (FEMF) tests
- Electronic speech detection
- Line in use tests (*Confirmation of busy where no speech is present*)
- Receiver off hook detection
- Intercept detection
- Denied service detection
- Direct Current (DC) tests (*An array of configurable DC resistance and voltage*)
- PBX identification
- Alternating Current (AC) signature identification
- An array of configurable AC impedance and voltage
- Longitudinal balance test
- Open detection and measurement
- Capacitive balance measurement
- Line circuit test
- Draw and Break dial tone test
- Soak test (*Tests to measure variation in DC resistance over time, to determine if a ground is “swinging” and it may be “dried out” by applying voltage)*
- Ringer test
- Length of loop measurement

5.7. INTEGRATED DLC TESTING - 5ESS

Figure 1•4 is an example of Integrated DLC Testing - 5ESS

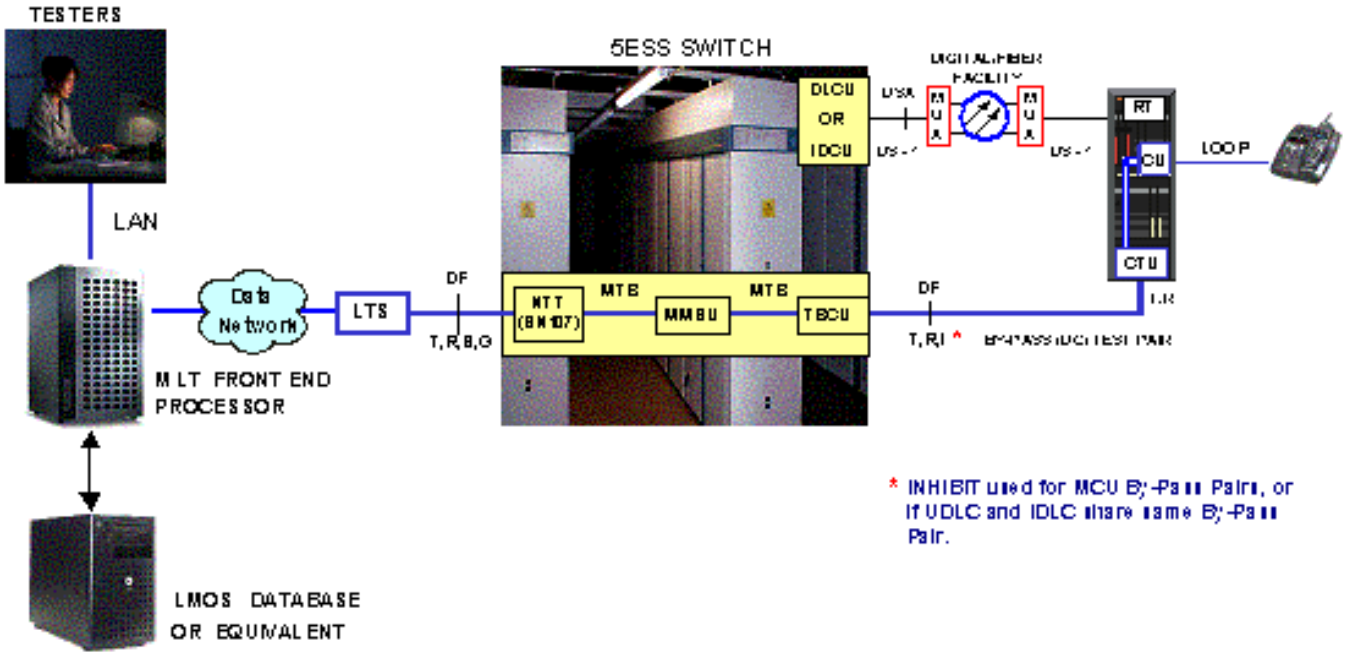


Figure 5•1 Integrated DLC Testing - 5ESS

5.8. INTEGRATED MLT - GENERAL

Only available in the 5ESS

- A switch unit called a Directly Connected Test Unit (DCTU) replaces LTS functionality.
- No-Test Trunks (NTTs) (via SN-107) are no longer required.
- Pair Gain Test Controller (PGTC) is still used when testing UDLC POTS, but it is wired differently.

- A Modular Metallic Service Unit (MMSU) provides the metallic path through the 5ESS.
- Provides enhanced **VER Codes**, i.e., DP and FJ.
- Major benefit to this configuration is cost.

5.9. INTEGRATED LOOPCARE/MLT MAJOR COMPONENTS

- Integrated LoopCare Datalink
- Directly Connected Test Unit (DCTU)
- Modular Metallic Service Unit (MMSU)
- Test Bus Control Unit (TBCU)
- Pair Gain Test Controller (PGTC)

5.10. INTEGRATED LOOPCARE/MLT DATALINK

- Utilizing Integrated LoopCare/DCTU, a datalink from LoopCare (via the DCN) is connected through a serial port directly on the switch IOP. It is through this datalink that the switch interprets test requests and sends the relevant commands to the DCTU.
- The Synchronous Data Link (SDL) supporting Integrated LoopCare will be “SDL2”. *(It may be viewed by accessing “OS Links”)*
- VCS Datakit or a leased-line may carry the Integrated LoopCare

datalink.

- The Integrated LoopCare datalink has an upper limit of 31 simultaneous accesses, although not probable, due to blocking considerations within the switch (available MMSU, DCTU or LU metallic resources).

5.11. DIRECTLY CONNECTED TEST UNIT (DCTU)

- Replaces the LTS in Integrated LoopCare.
- Because it is a switch unit, it is provisioned and maintained using the 5ESS ODD, diagnostics and personnel.
- The DCTU is comprised of:
  - DCTU common control (DCTUCOM) circuit
    - The DCTUCOM interfaces a PICB for communication
- The Equipment Access Network (EAN). *(The EAN allows any of the three possible PMU shelves to connect to any of the twelve possible MTBs.)*
- One to three Precision Measuring Units (PMUs). *(Four, eight or twelve MTB ports (Four per PMU.))*
- In order to reduce blockages:
  - **VER B0** - Test Equipment Busy
  - **VER BG** - No MAB Available
  - **VER BE** - No MTIB Available.
- The twelve DCTU (MTB) ports should be connected, one per MMSU Service Group (SG). Even numbered DCTU ports are wired to SG0, and odd numbered DCTU ports are wired to SG1.

5.12. MODULAR METALLIC SERVICE UNIT – MMSU

- The MMSU represents the internal metallic switching network within the 5ESS. *(Up to 5E11, each MMSU may have up to four shelves (0-3) with a SG 0 and SG 1 in each shelf.)*
- The MMSU offers metallic service circuits for 5ESS use:
  - Signal Distributors - SD (TN221)
  - Scan points - SC (TN220)
  - Metallic Access - MA (TN138)
  - Metallic Test Interconnection Bus Access - MTIBAX (TN138)
  - Automatic Line Insulation Test - ALIT (TN328)
  - Distribution Frame Test Access Circuit - DFTAC (TN1040)
  - Gated Diode Crosspoint Compensator - GDXC (TN880).

5.13. EXAMPLE OF MMSU SHELF 0 CIRCUIT PACKS

The following table is an example of the MMSU Shelf **0** Circuit Packs divided into Service Groups **1** and **0**.

Table 5•4 MMSU Shelf 0 Circuit Packs

	Pack	Type	Location	
	TN138	MTIBAX	178	
	TN1040	DFTAC	170	
	TN328	ALIT	162	
	TN880	GDXC	154	
	TN221	SIG DIST	146	
SAME AS SERVICE	TN220	SCAN	138	SERVICE
GROUP 0	TN880	GDXC	130	GROUP 1
	TN138	MA	122	
	TN138	MA	114	
	TN879	COM	106	
	494LA	PWR UNT	098	
	TN138	MTIBAX	090	
REQUIRED FOR MDF TESTING	TN1040	DFTAC	082	
REQUIRED FOR ALIT	TN328	ALIT	074	
	TN880	GDXC	066	
REQUIRED FOR PGTC/TBCU	TN221	SIG DIST	058	SERVICE
	TN220	SCAN	050	GROUP 0
	TN880	GDXC	042	
REQUIRED WHEN MTBs EXCEED 15	TN138	MA	034	
	TN138	MA	026	
	TN879	COM	018	
	494LA	PWR UNT	010	

5.14. MMSU Metallic Service Circuits for 5ESS Use:

5.14.1. SIGNAL DISTRIBUTOR – SD (TN221)

- **Software-accessible relay points used by the 5ESS to metallically "signal" an event or request.**
- **Can be manually manipulated (turned on or off) with the input command EX:DISTPT.**
- **Used for many functions including:**
  - o **Sleeve lead control for the Integrated LoopCare connection to the PGTC.**
  - o **Signaling control to the TBCU when testing Integrated LoopCare.**

5.14.2. SCAN POINT – SC (TN220)

- Software-readable circuits used by the 5ESS to metallically "sense" an event or request
- Status can be manually read with the input command OP:MSUSP
- Used for many functions, including Inhibit lead (I-lead) sensing through the TBCU when testing IDLC.

5.14.3. METALLIC ACCESS – MA (TN138)

- Contains 16 Metallic Test Bus (MTB) ports:
  - Fifteen (0-14) are available for MTB connection to 5ESS SM units
  - Sixteenth port (15) is dedicated for internal MMSU diagnostics.
- Functions as a 16x4 metallic matrix (16 MTB ports to 4 MMSU junctors (MABs))
- Because only four junctors are available per MMSU SG, they can easily cause test blockage. The MTBs to the MA ports must be assigned (spread out through the MMSU) to reduce the demand for junctors. This will help to prevent:
  - **VER B0** (Test Equipment Busy)
  - **VER BG** (No MAB Available).
- Is diagnosable either by control/display poke commands or input command DGN:MA.
  - Phase 1: Tests the MA communication and relay drivers.
  - Phase 2: (102) Tests the MTBs out to connected SM units (internal diode protocol test).
  - Phase 3: (103) Diagnostic - Tests the by-pass pair connection from the TBCU to the IDLC RT CTU/MTAU.
- Can have up to three TN138 packs per MMSU SG, allowing for up to 45 MTB ports per MMSU SG.
- Are provisioned within slots 026, 034, and 042 in SG0 and slots 114, 122 and 130 in SG1.

5.15. Metallic Test Interconnection Bus Access - MTIBAX (TN138)

- Contains 16 Metallic Test Bus Access ports called Metallic Test Interconnection Bus (MTIB) ports.
  - o Fourteen (0-13) are used for metallic interconnections between MMSUs.
  - o Last two ports (14-15) are used for internal MMSU diagnostics.
- Provisioned within slots 090 in SG0 and 178 in SG1.
- The 5ESS supports a maximum of 14 MTIBs for metallic interconnections between MMSUs:
  - o Assignment of MTB ports on the MAs should be engineered to highlight the use of MTIBs
  - o This will help to prevent:
    - § **VER B0** - Test Equipment Busy
    - § **VER BE** - No MTIB Available.

5.16. Automatic Line Insulation Test - ALIT (TN328)

- Used as the simple tester for night routine ALIT testing.

5.17. Distribution Frame Test Access Circuit - DFTAC (TN1040)

- Used as the DCTUs interface to an MDF test “shoe” for Integrated LoopCare testing of non-assigned cable pairs, or some switched specials.

5.18. Gated Diode Crosspoint Compensator - GDXC (TN880)

- Utilized whenever metallic testing occurs through a Line Unit (LU)
- Designed to compensate for minute leakages to ground that occur on the gated crosspoint diode (GDX) with an LU.
  - o A GDXC is a solid-state circuit that emulates a relay.
  - o This solid-state circuit has minute leakages to ground that do not affect voice or data circuits, but are detrimental to metallic testing.
  - o The GDXC is switched into the metallic test to compensate for the leakages.
- To help prevent:
  - o **VER B0** - Test Equipment Busy
  - o **VER BC** - No GDXC Available.
- A minimum of two GDXC packs should be assigned to each service group where DCTU ports reside.

5.19. MODULAR METALLIC SERVICE UNIT - MMSU

Figure 5•2 is an example of Modular Metallic Service Unit – **MMSU**.

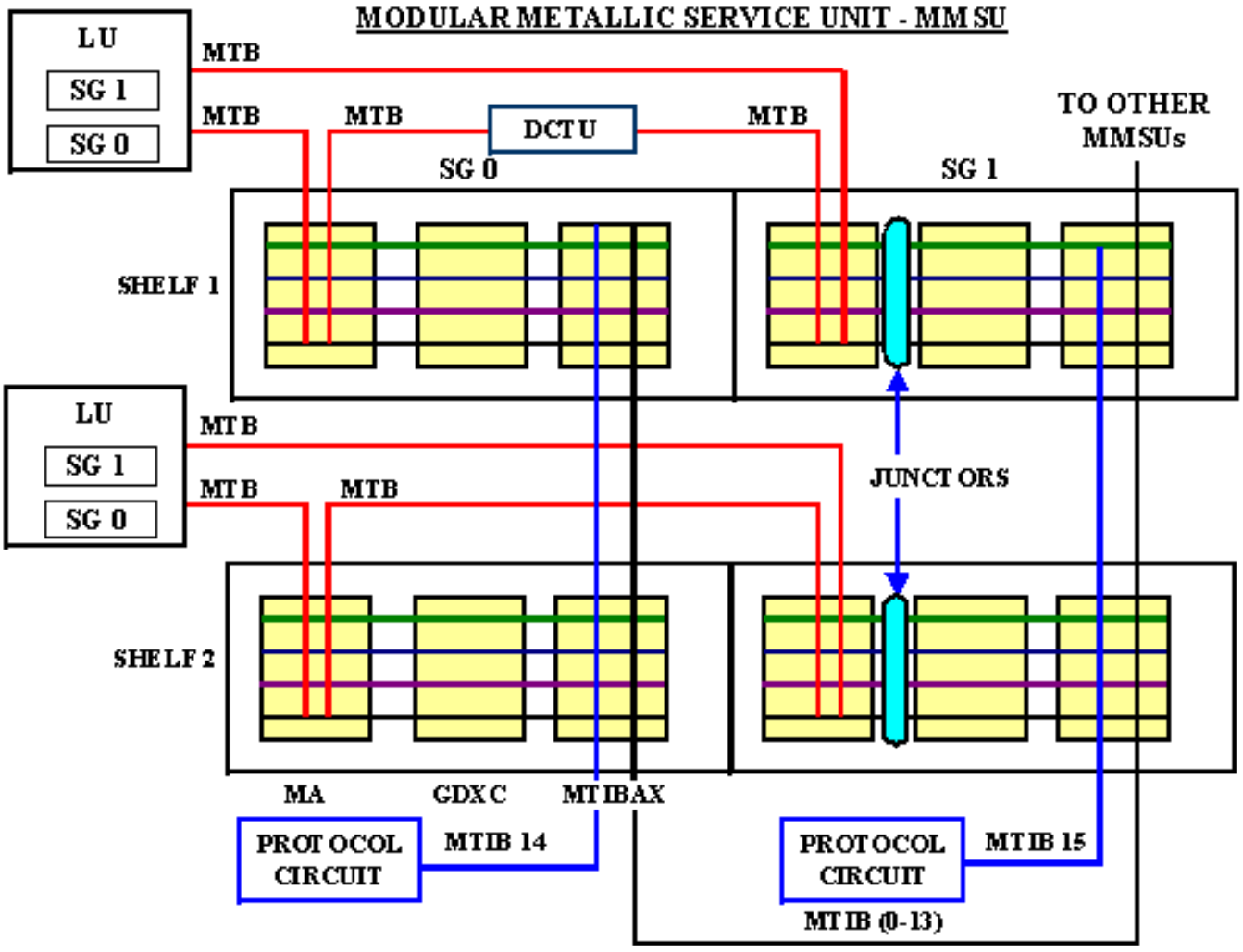


Figure 5•2 Modular Metallic Service Unit - MMSU

5.20. TEST BUS CONTROL UNIT (TBCU) SHELF

Figure 5•3 is an example of a Test Bus Control Unit (**TBCU**) Shelf.

Figure 5•3 Test Bus Control Unit (TBCU) Shelf

5.21. TEST BUS CONTROL UNIT – TBCU

- Metallic test interface for Integrated DLC testing within the 5ESS switch.
- Each TBCU shelf can house 15 Bus Unit circuit packs (SM500):

- o One SM500 circuit pack for every two Metallic Test Pairs (MTB) serving Remote Terminal (RT) locations
- o Each SM500 pack can support two test ports (DC test pairs **A** and **B**) for tests out to two separate RT sites.

- A TBCU shelf can support 30 RT sites:
  - o 15 SM500 packs x two test ports per SM500 pack
  - o One or both circuits may be utilized on an SM500.
- Each Metallic Test Path (MTP) can accommodate **10** co-located Integrated SLC RTs if LoopCare is used.
- Each MTP may be shared between Integrated and Universal SLC systems. *(All SLC RTs that share an MTP must be co-located.)*
- If all RTs on an MTP are Universal SLC terminals, no TBCU test circuits are required. *(TBCU test circuits are required only when some or all terminals on an MTP are Integrated SLC terminals.)*
- The seven-pair input appearance of the TBCU test port is connected to:
  - o One MTB pair
    - § Defined in **RCV 18.12**
    - § Defined in **RCV 18.10** if DCLU-fed
    - § Defined in **RCV 18.15** if IDCU/DNUS-fed
  - o One Scan Point pair defined in **RCV 18.12**
  - o Five Signal Distributor pairs defined in **RCV 18.12.**

5.22. TBCU Assignment Rules

- Scan **(SC)** Points:

- Each bus unit circuit (two per SM500) requires one scan point:
  - Assign **A** circuit scan terminations to MMSU service group **0** scan points.
  - Assign **B** circuit scan terminations to MMSU service group **1** scan points.
- Scan point **31** **CANNOT** be used for TBCU use.

- Signal Distributor (SD) Points:
  - Each bus unit circuit (two per SM500) requires five SD points:
    - Assign **A** circuit SD terminations to MMSU service group **0** SD points.
    - Assign **B** circuit SD terminations to MMSU service group **1** SD points.
  - All SD points associated with a TBCU must be assigned to the same scan pack on the same MMSU shelf service group.

- Metallic Test Bus (MTB):
  - Each bus unit circuit (two per SM500) requires one MTB:
    - Assign **A** circuit MTB terminations to any available MMSU service group **0** MTB point.
    - Assign **B** circuit MTB terminations to any available MMSU service group **1** MTB point.

NOTE: Diode terminations required for MTBs in the idle state are provided by the TBCU for those MTBs associated with it.

5.23. TBCU Wiring

Figure 5•4 is an example of TBCU Wiring.

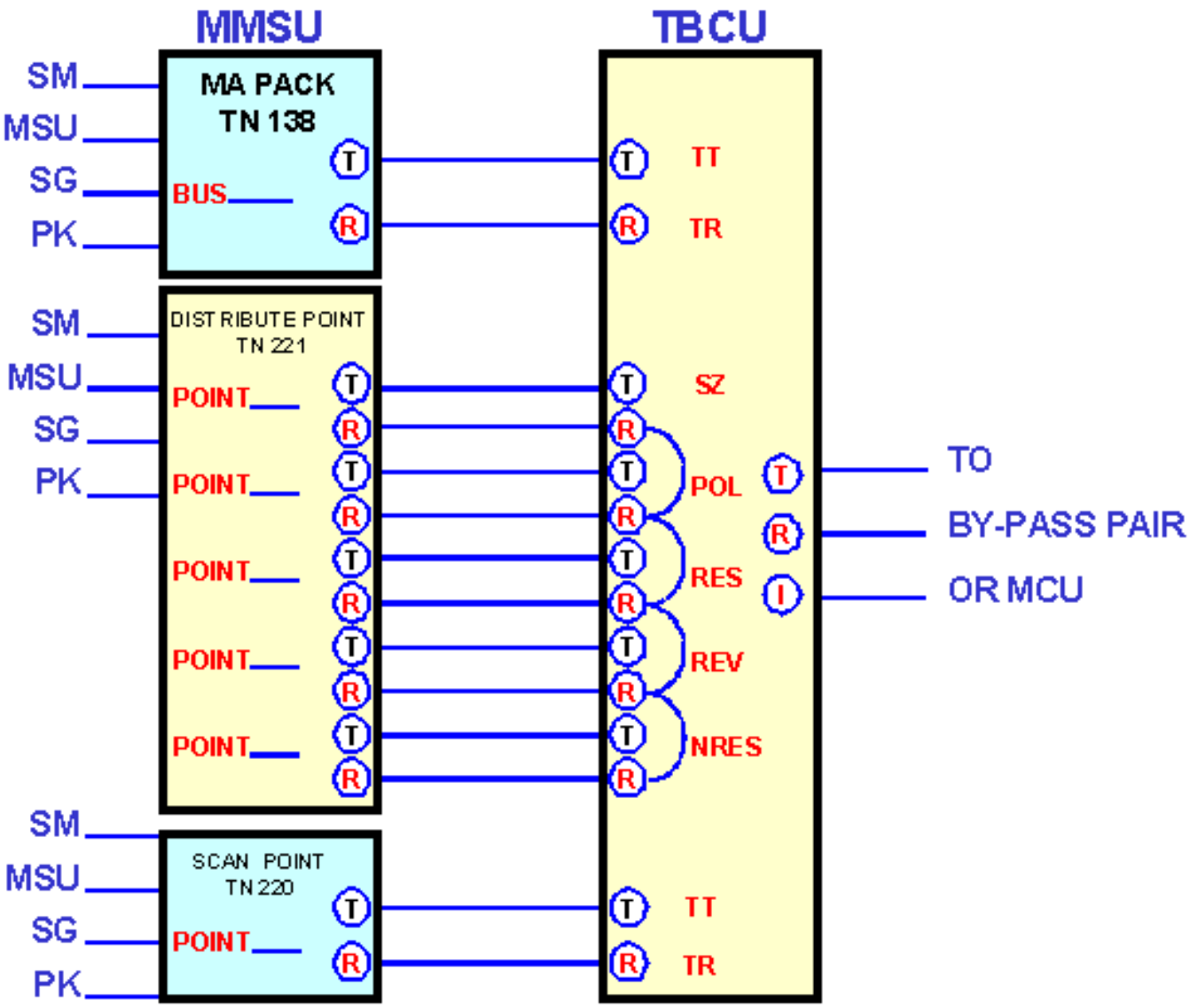


Figure 5•4 TBCU Wiring

5.24. TBCU – FOUR MAJOR FUNCTIONS

1. To provide a 56 Kohm “delta” signature:

   - o To inform LoopCare (by the measurement of the DCTU) that the line under test is served by IDLC
   - o 56 Kohm Tip to Ground (GND)
   - o 56 Kohm Ring to GND
   - o 56 Kohm Tip to Ring.

1. To remove the 56 Kohm signature and apply a 1Kohm Tip-GND on the TBCU port:

   - o To indicate that metallic access is successful
   - o The DCTU then applies 117 volts on the Tip side of the TBCU port which (if metallic access was successful) will go through the 1 Kohm Tip-GND, indicating to the DCTU/LoopCare that metallic access is successful.

2. To remove the 1 Kohm Tip-GND and switch the DC test pair to the assigned MTB (**RCV 18.10** or **RCV 18.15**) *(The DCTU then proceeds to make the metallic test.)*

3. To relay the results of the channel test made by the TTF by placing signatures on the assigned MTB for the DCTU to read:

   - o In IDLC testing, the channel test is performed by the TTF in the GDSU in order to help prevent:
     - § **VER 05** - Test OK - Channel Not Tested

- § **VER 55** - Channel Status Not Identified.

o In UDLC testing, the channel test is performed by PGTC.

5.25. Recent Change Views

5.29.1 Recent Change View 18.10

Figure 5•5 is an example of 5ESS Recent Change 18.10.

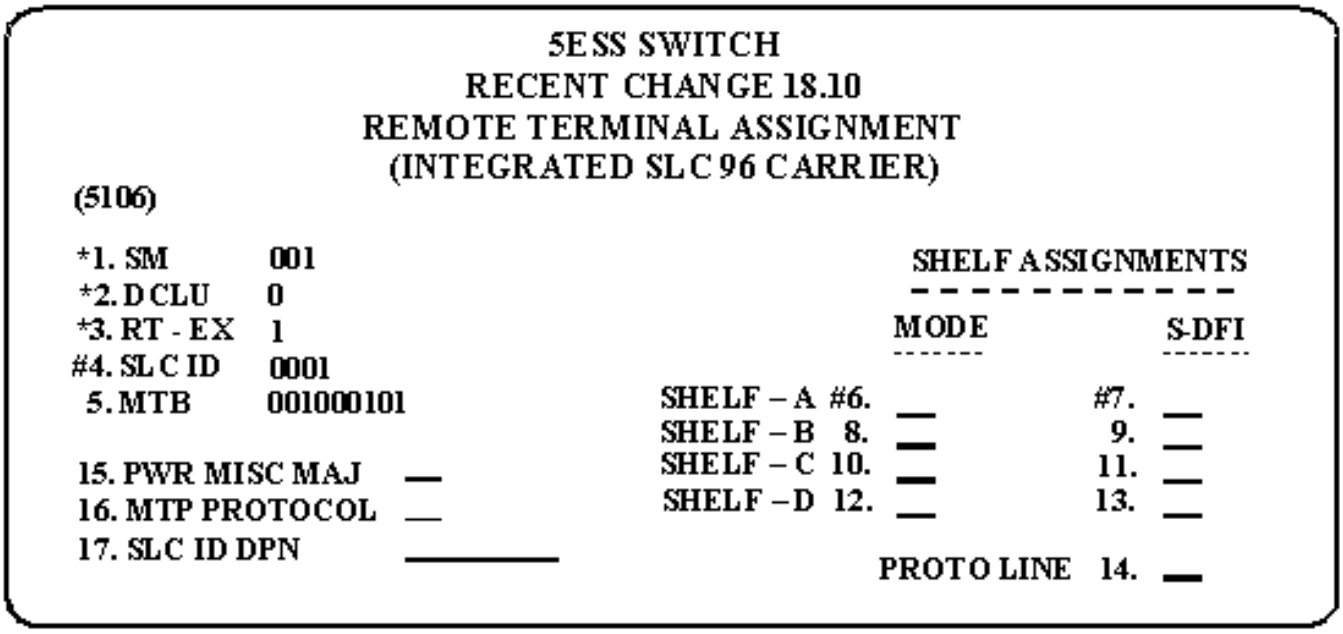


Figure 5•5 5ESS Recent Change 18.10

5.29.2 Recent Change View 18.15

Figure 5•6 is an example of 5ESS Recent Change 18.15:

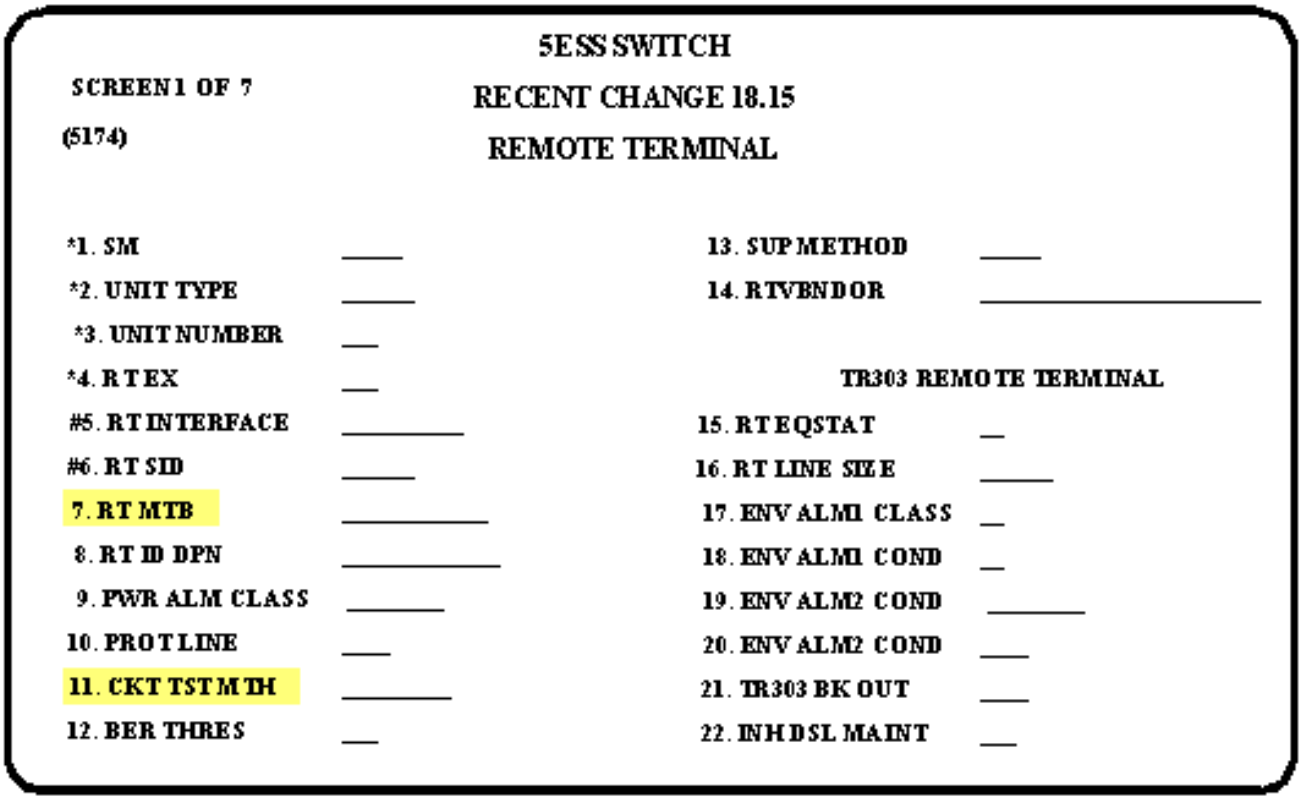


Figure 5•6 5ESS Recent Switch Recent Change 18.15

5.29.3 Recent Change View 18.15

Figure 5•7 is an example of 5ESS Recent Change 18.12.

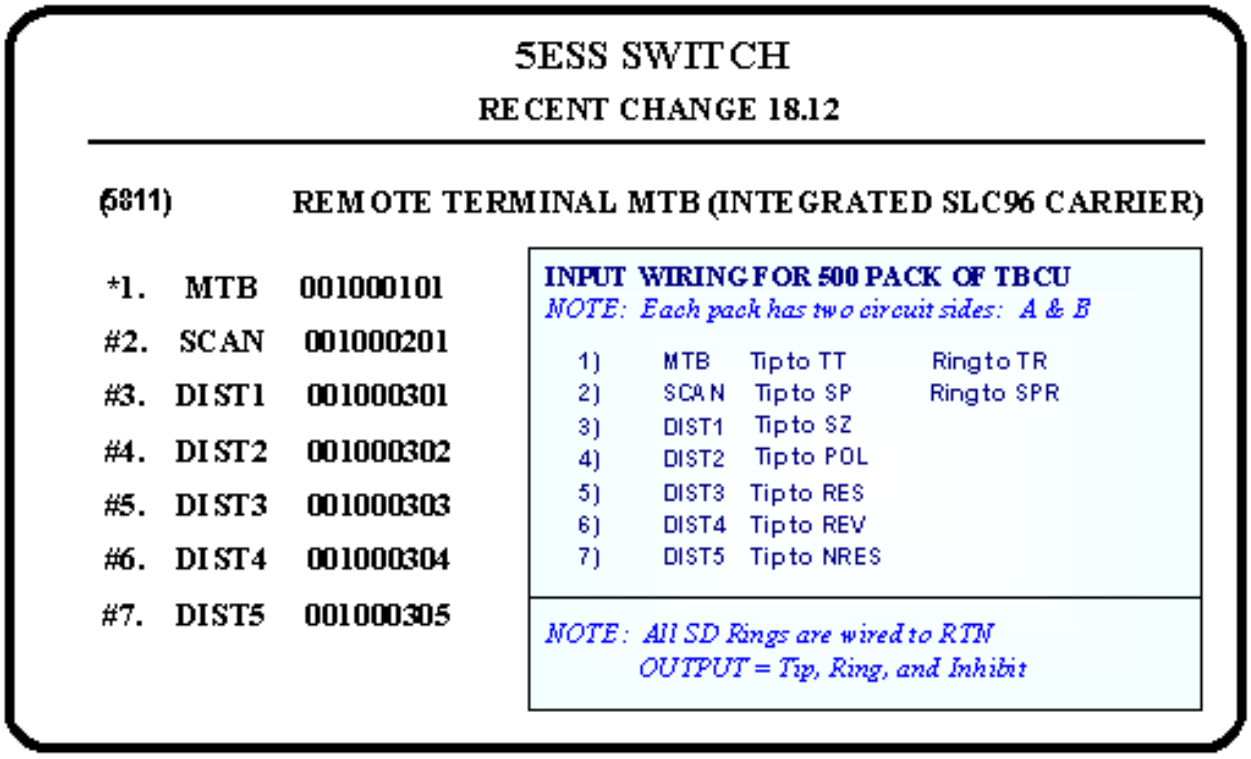


Figure 5•7 5ESS Switch Recent Change 18.12

5.26. PAIR GAIN TEST CONTROLLER – PGTC

Figure 5•8 is an example of the Pair Gain Test Controller (PGTC).

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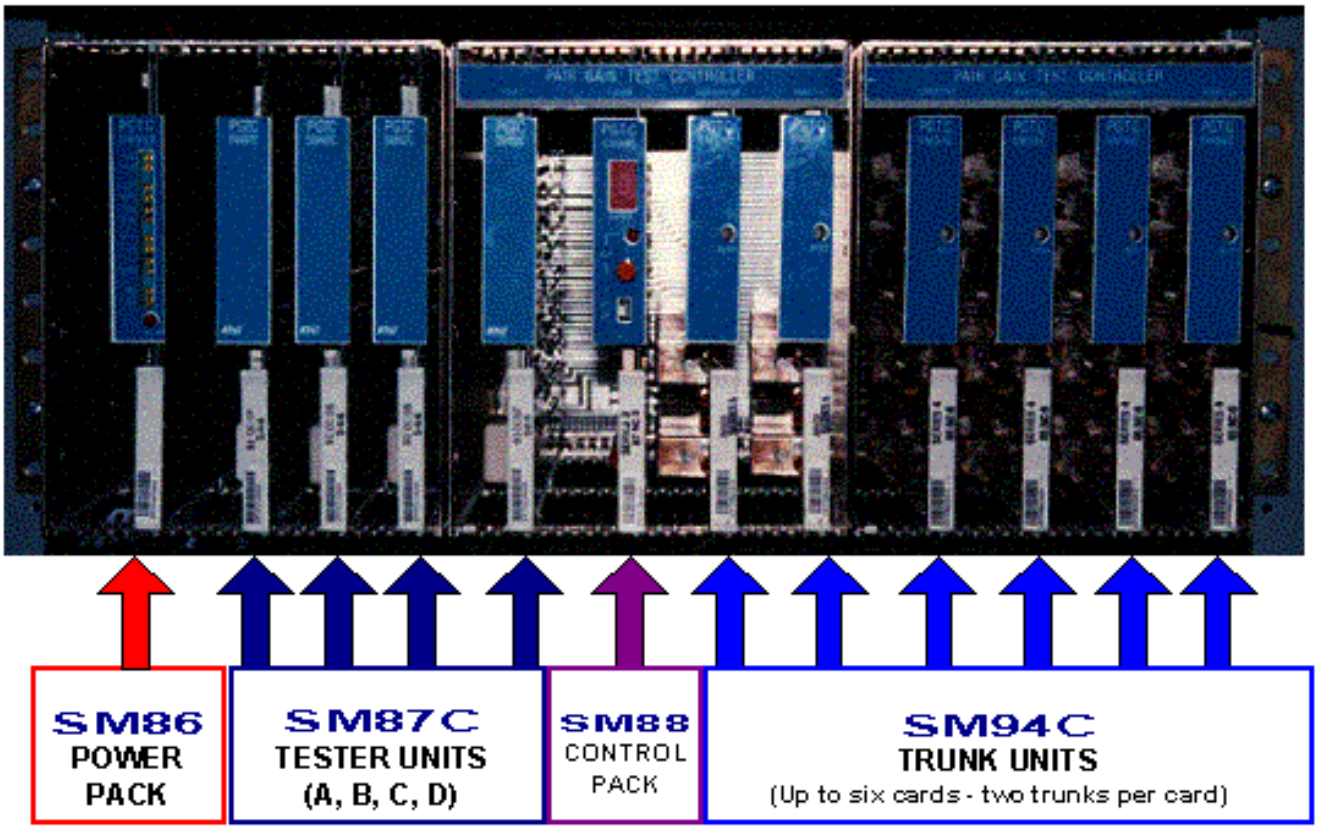


Figure 5•8 Pair Gain Test Controller - PGTC

5.30.1 PAIR GAIN TEST CONTROLLER

- Provides metallic path by cutting through metallic test pair (*or emulated metallic test pair using MCU® units*) from CO to RT
- Wired between Test System (LTS) and NTT *(One shelf accommodates up to 12 NTTs)*
- One control shelf per office; expansion shelf can be added if needed.
  - o Control shelf requires –48 volts DC (*signal grade*) at 2.5 Amperes (*maximum*) and uninterrupted ringing voltages at 0.5 Amperes (*maximum*).
  - o Ringing should be 86•100 VAC 20Hz with •42.5 to 52.5 Vdc superimposed. Pin 10 on back of PGTC.
- In Integrated LoopCare, the PGTC does not interface with an NTT because the NTT is not used.

- Each assigned PGTC port “input” side (leads TT, TR, TS) is connected to one dedicated MTB and two dedicated SD points (that are connected to 1100 ohm and 3650 ohm resistors).
  - The two SD points will emulate the sleeve lead of an NTT. This emulated “TS” sleeve lead (*input side*) is required by the PGTC for port control.

- Each corresponding “output” side (leads T, R) PGTC port is connected to another dedicated MTB. The Sleeve lead is not needed and thus not connected.
- **RCV 14.7** configures the required MTBs and SDs for each assigned port.

5.27. PGTC - REQUIREMENTS SPECIFIC TO 5ESS

- Only one PGTC test port will terminate on an MMSU shelf service group.
- Two SD points are required for each PGTC. *(These points must be assigned sequentially to the same MMSU and the same SD circuit pack.)*
- Two MTBs are required per PGTC port:
  - These must be assigned sequentially to the same MMSU and the same metallic access circuit pack.
  - A minimum of one MTB assigned to the DCTU must terminate on the same MMSU shelf service group as the two MTBs assigned to the PGTC port.
- A PGTC test port must terminate on each MMSU shelf service group where the MTB for a DCTU port *(used in testing Universal SLC-96 RTs)* terminates.
  - An optional connection:

§ The PGTC can be connected in series with the DCTU and MMSU by connecting an MTB from DCTU PMU port via the DF to “MTB IN” on PGTC

§ Then connect “MTB OUT” from PGTC via the DF to MMSU.

o An optional connection: When Universal SLC is present in the 5ESS switch, a minimum of one PGTC is needed on each MMSU for testing Universal SLC lines.

§ This configuration may be accepted in an office with a minimum number of Universal SLC lines. If Universal SLC testability is down with this configuration, the office may need to add additional PGTC access to their MMSU.

NOTE: that PGTC needs to be on the same shelf service group as the DCTU PMU port RCV 20.9.

5.28. MDF Wiring for PGTC Ports

Figure 5•9 is an example of MDF Wiring for PGTC Ports.

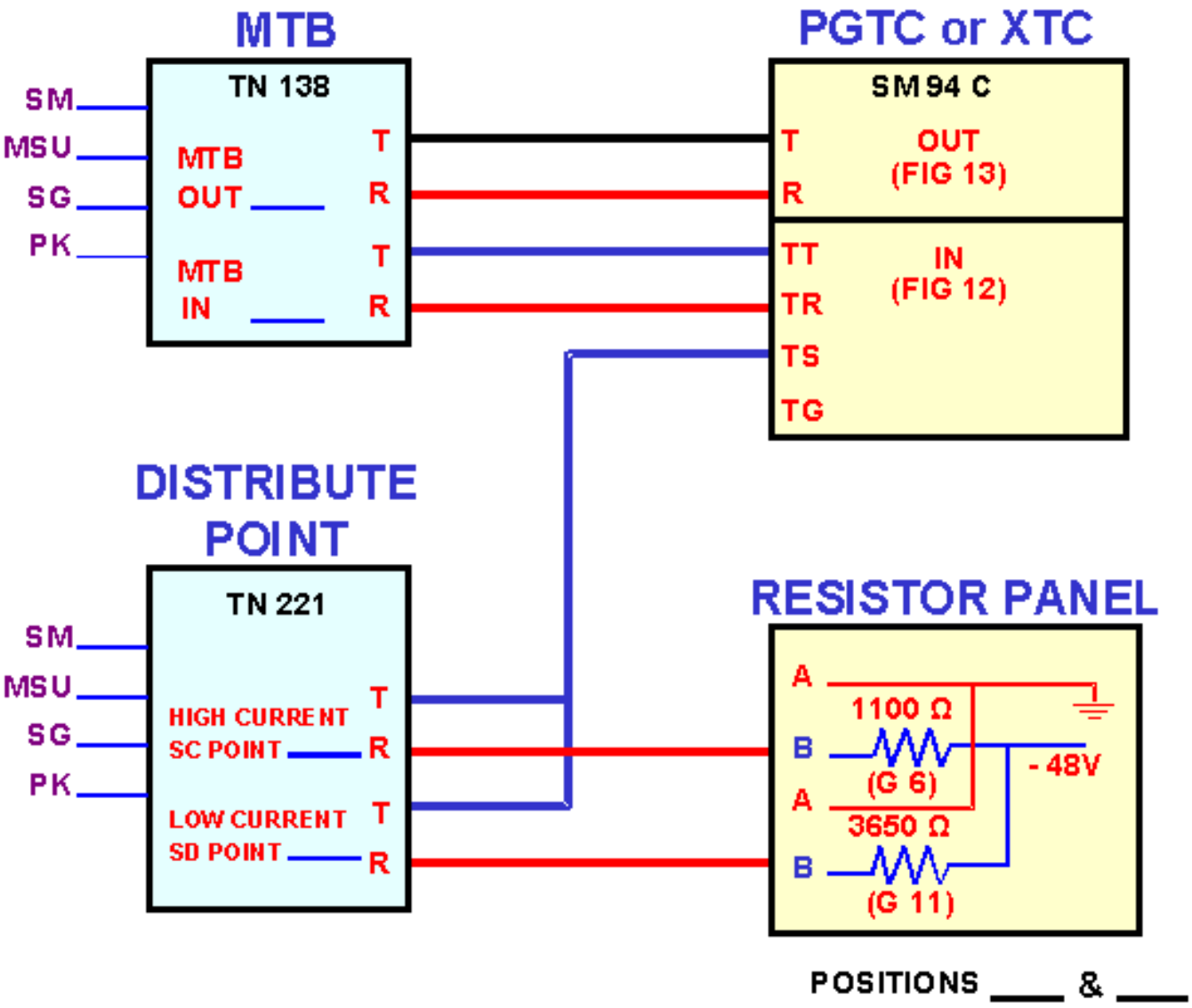


Figure 5•9 MDF Wiring for PGTC Ports

5.29. Recent Change View 14.7

MTB And **DIST** Points Are Assigned On **Recent Change View (RCV) 14.7**

The following diagram Figure 5•10 page 5•28 is an example of 5ESS Recent Change 14.7:

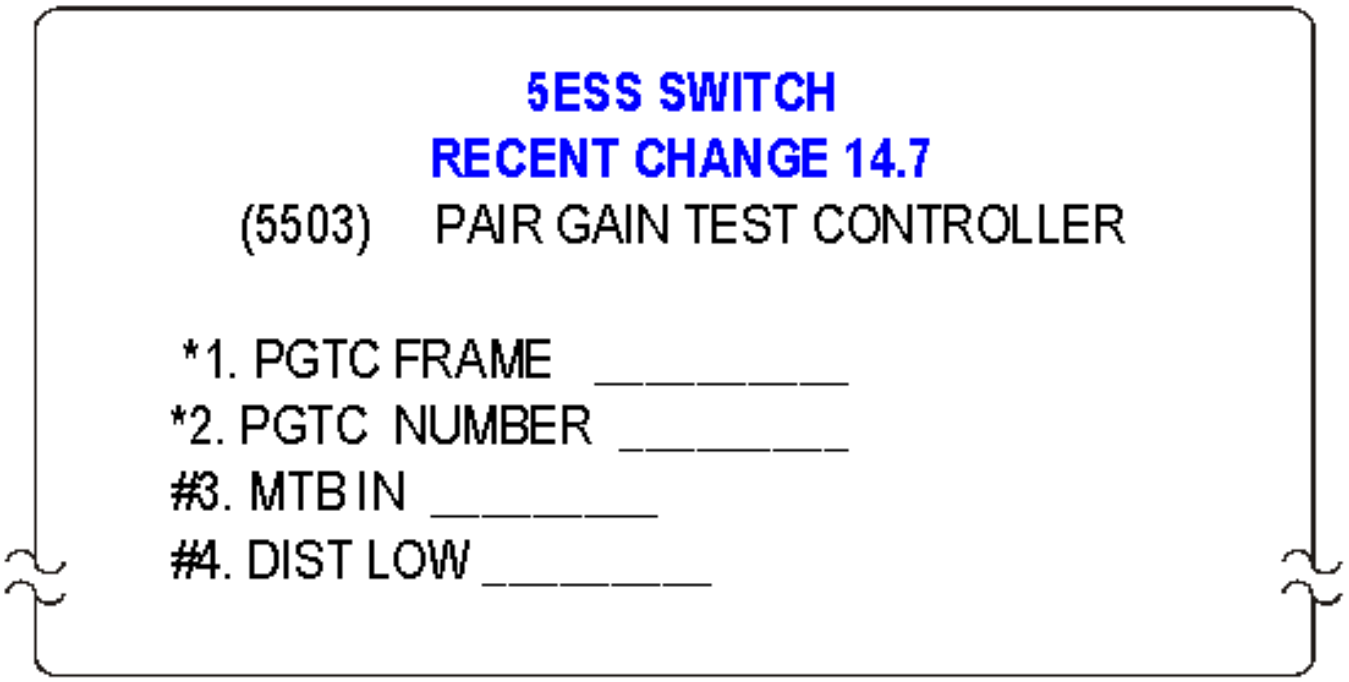


Figure 5•10 MTB and DIST Points

5.30. RCV 14.7 CONTROLLER RECORD

The following table is an example of the RCV 14.7 Controller Record.

Table 5 RCV 14.7 Controller Record

PGTC FRAME	PGTC NUMBER	MTB IN	DIST LOW		PGTC FRAME	PGTC NUMBER	MTB IN	DIST LOW
1	1	001000113	001000600					
1	2	001010113	001010600					
1	3	001000912	001001404					
1	4	001010912	001011404					
1	5	003000010	003000400					
1	6	003010010	003010400					
1	7	003001008	003001402					
1	8	003011008	003011402					
1	9	003001610	003001808					
1	10	003011610	003011808					

RCV 14.7 - FIELD: PGTC NUMBER

- Represents a **PGTC** port. Each assigned **PGTC** port has its own unique **PGTC NUMBER** and **RCV 14.7** view.

RCV 14.7 - FIELD: MTB IN

- Represents the **MTB** to be connected to the "**input**" side **TT** and **TR** leads of the **PGTC** port.
- The "**MTB OUT"** that connects to the "**output**" side **T** and **R** leads of the corresponding **PGTC** port is not displayed within the View. It is automatically sequentially assigned to the next **MTB** from "**MTB IN**".
- "**MTB OUT = 1 + MTB IN**" - consequently, "**MTB IN**" must be assigned an **MTB** that has the next sequential **MTB** unassigned.

RCV 14.7 - FIELD: DIST LOW

- Represents the **SD** point connected to the **3650-ohm** resistor.
- Used to emulate the low sleeve current condition.
- Higher resistance equates to lower current **48/3650=13Ma**

5.31. QUESTIONS

1. What hardware is required for DLC testing of 5ESS?

2. On an IDCU fed IDLC what recent change view contains the test path information?

3. With the integrated MLT what recent change view contains the PGTC information?

SECTION 6 iNTEGRATED DLC TESTING DMS•100

In this Section:

6.1. objectives

The student will understand the hardware and software required for IDLC testing in Nortel's DMS-100 switch.

6.2. DMS-100 – IDLC Testing Overview

- The DMS-100 switch has IDLC capability.
- The DMS-100 also uses a Metallic Test Access (MTA) circuit (similar to the MSU), Subscriber Multiplexer SLC 96 (SMS) interfaces (similar to DCLUs or IDCUs), and Pair Gain Applique (similar to the TBCU).

Figure 4•2 is an example of the DMS-100 – IDLC Testing Architecture.

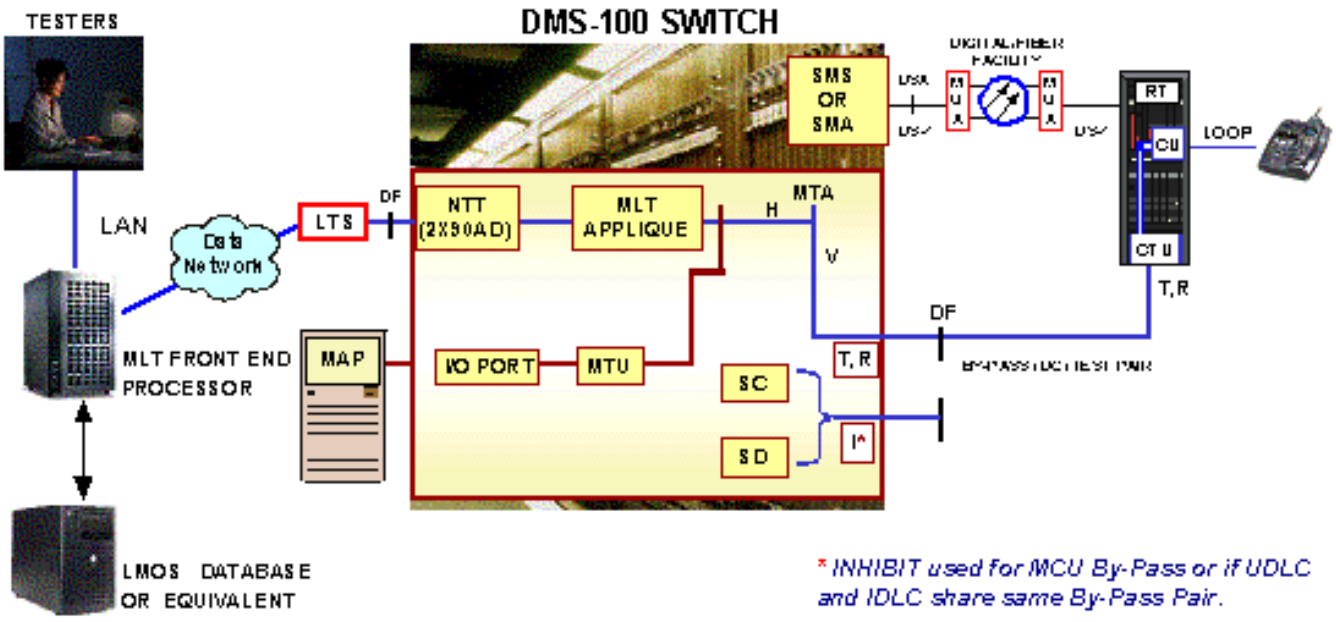


Figure 6•1 DMS-100 – IDLC Testing Architecture

6.3. DMS-100 – UDLC/IDLC Testing Architecture

Figure 4•3 is an example of the DMS-100 – UDLC and IDLC Testing Architecture.

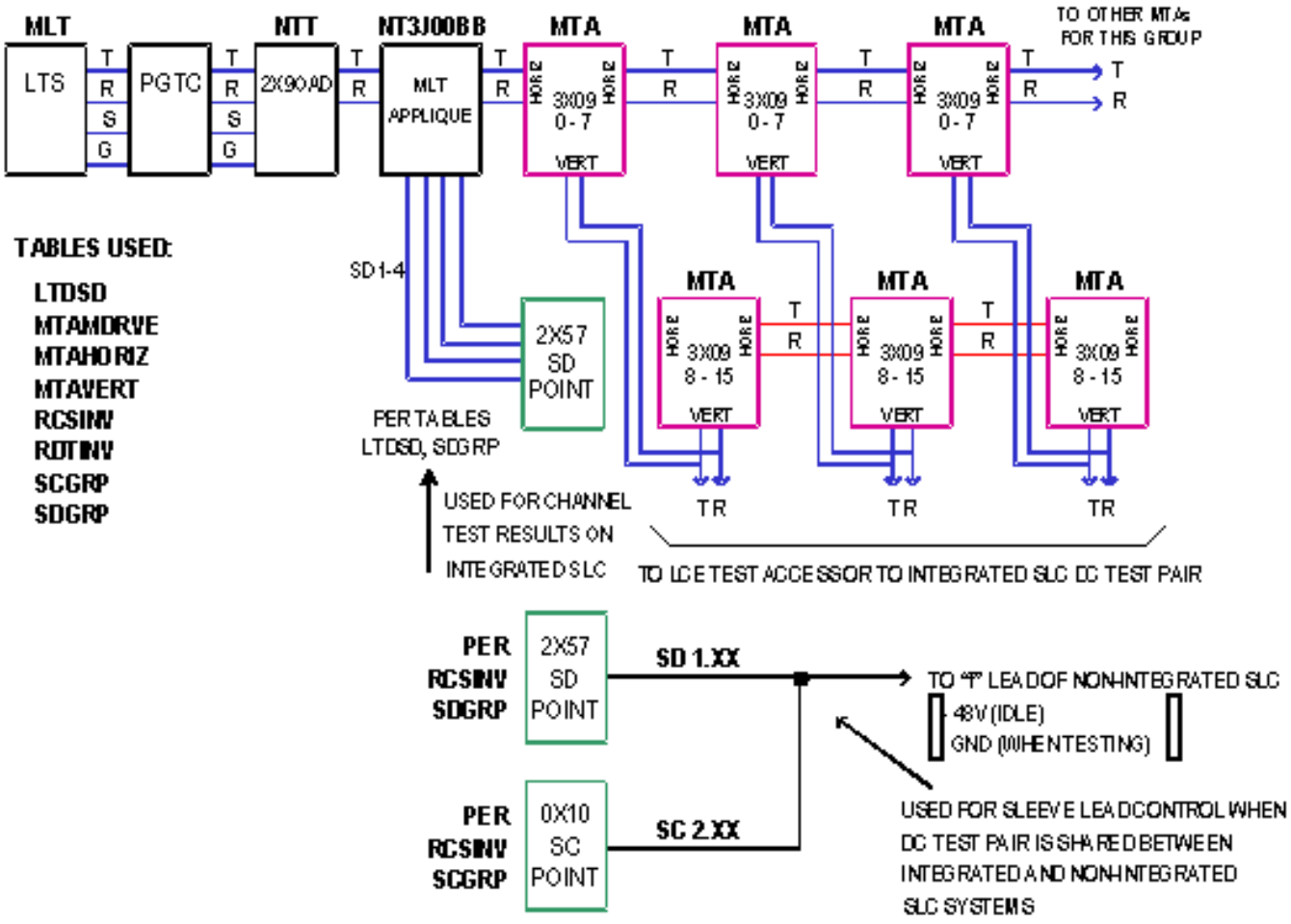


Figure 6•2 DMS-100 – UDLC and IDLC Testing Architecture

6.4. DMS-100 –

Figure 6•3 is an example of

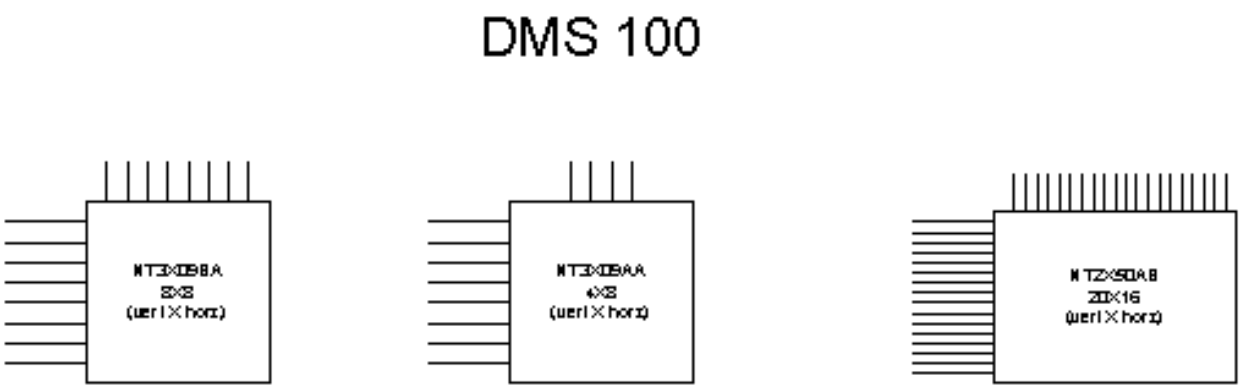


Figure 6•3 DMS-100

6.5. MTA VERTICAL AND HORITZONTAL

Figure 6•4 is an example of

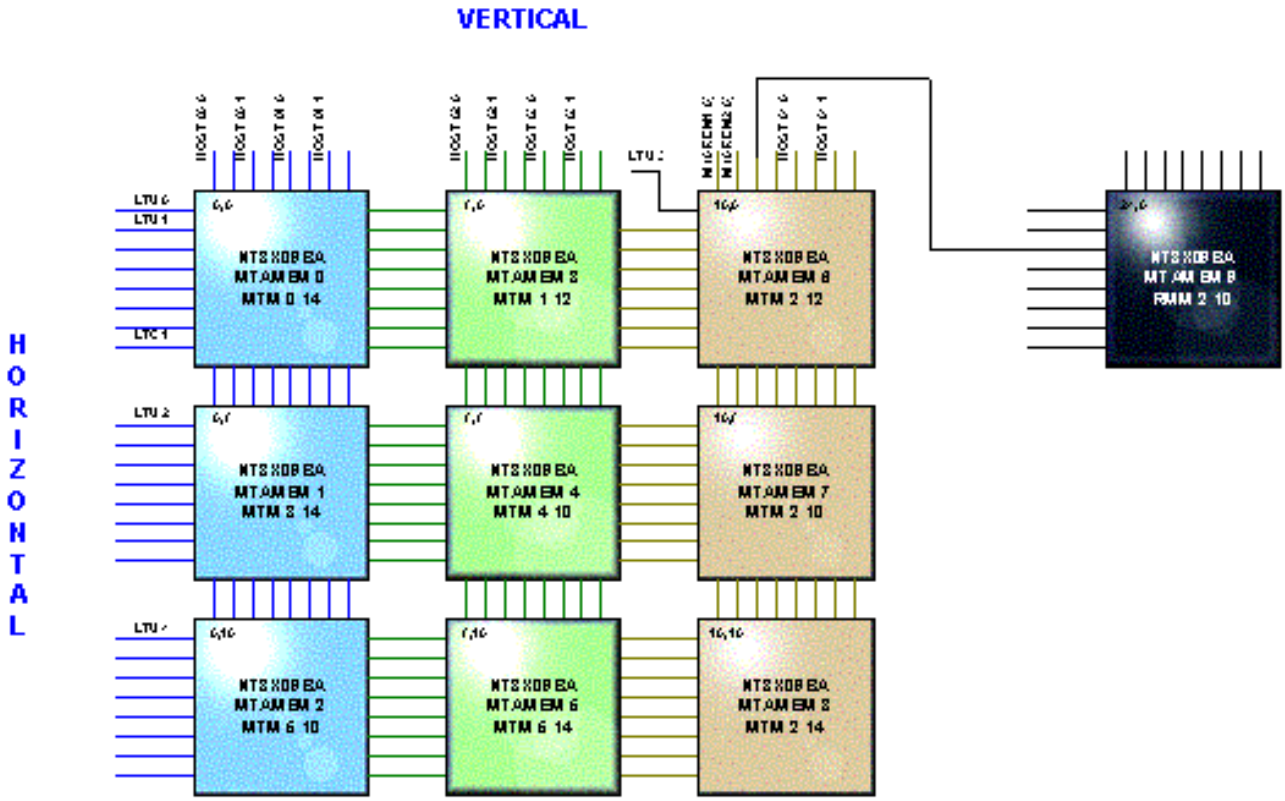


Figure 6•4 Horizontal and Vertical DMS-100

6.6. MTA EXAMPLE TABLES

Table 6 MTA Example Tables

MTA Example Tables

TABLE: MTAMDRVE

TOP

MTAMEM	VERT	HORIZ	TMTYPE	TMNO	TMCKTNO	MTACARD
0	0	0	MTM	0	14	3X09BA
1	0	8	MTM	3	14	3X09BA
2	0	16	MTM	5	10	3X09BA
3	8	0	MTM	1	12	3X09BA
4	8	8	MTM	4	10	3X09BA
5	8	16	MTM	5	14	3X09BA
6	16	0	MTM	2	12	3X09BA
7	16	8	MTM	2	10	3X09BA
8	16	16	MTM	2	14	3X09BA
9	24	0	RMM	2	10	3X09BA

TABLE: MTAVERT

TOP

VERT		VERTCONN
0		S L HOST 00 0
2		S L HOST 00 1
4		S L HOST 01 0
6		S L HOST 01 1
8		S L HOST 02 0
10		S L HOST 02 1
12		S L HOST 03 0
14		S L HOST 03 1
16	M (0 REM1 0)	
17	M (0 REM2 0)	
18		S E 2 0
20		S L HOST 04 0
22		S L HOST 04 1

TABLE:MTAHORIZ

TOP

HORIZ	HORIZGRP		HORIZAGT	MTAGRP
0	0	L	LTU 0 Y	(0 0) (3 0)
0	1	L	LTU 3 Y	(6 0)
1	0	L	LTU 1 Y	(0 1) (3 1) (6 1)
2	0	E	18	(9 2)
7	0	T	HOSTLTC 1	(0 7) (3 7) (6 7)
8	0	L	LTU 2 Y	(1 0) (4 0) (7 0)
16	0	L	LTU 4 Y	(2 0) (5 0) (8 0)

6.7. Typical Maintenance Trunk Module (MTM) Shelf (NT2X58)

Figure 6•5 is and example of a Typical Maintenance Trunk Module (MTM) Shelf (NT2X58).

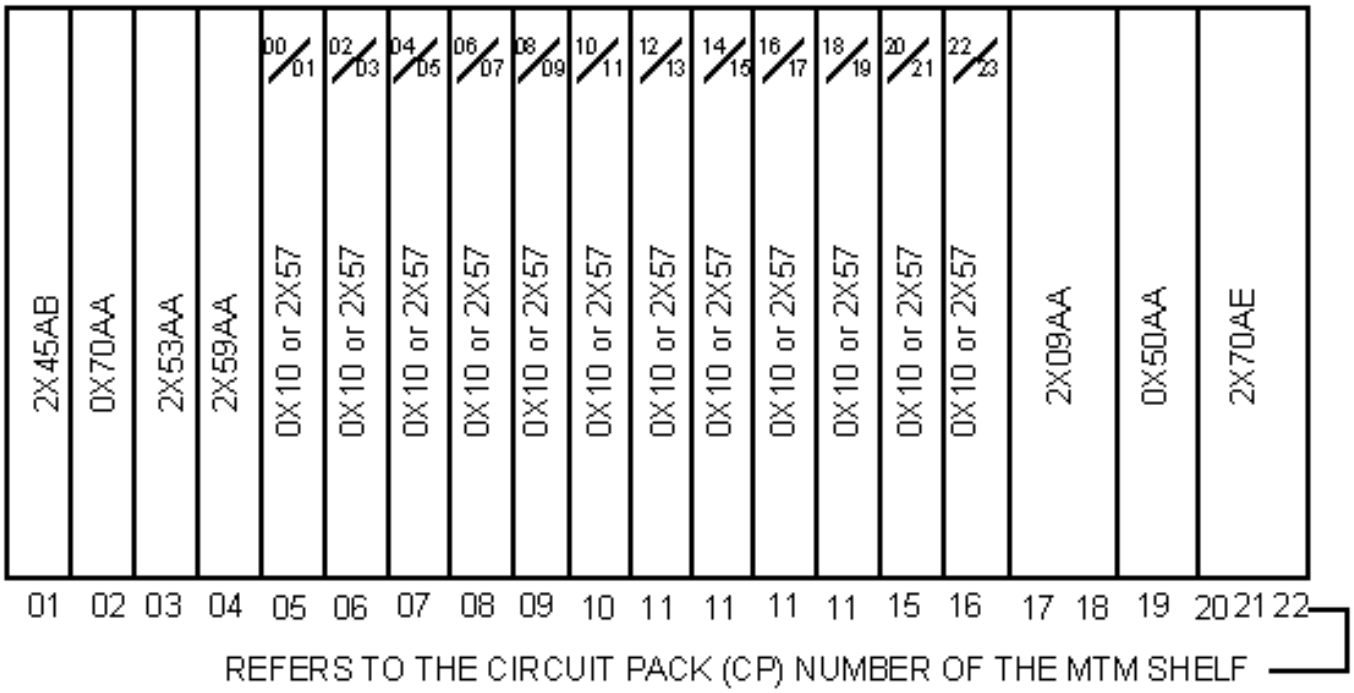


Figure 6•5 Typical Maintenance Trunk Module (MTM) Shelf (NT2X58)

6.8. Typical Integrated Services Module (ISM) Shelf (NTFX4101)

Figure 6•6 is and example of a Typical Integrated Services Module (ISM) Shelf

(NTFX4101).

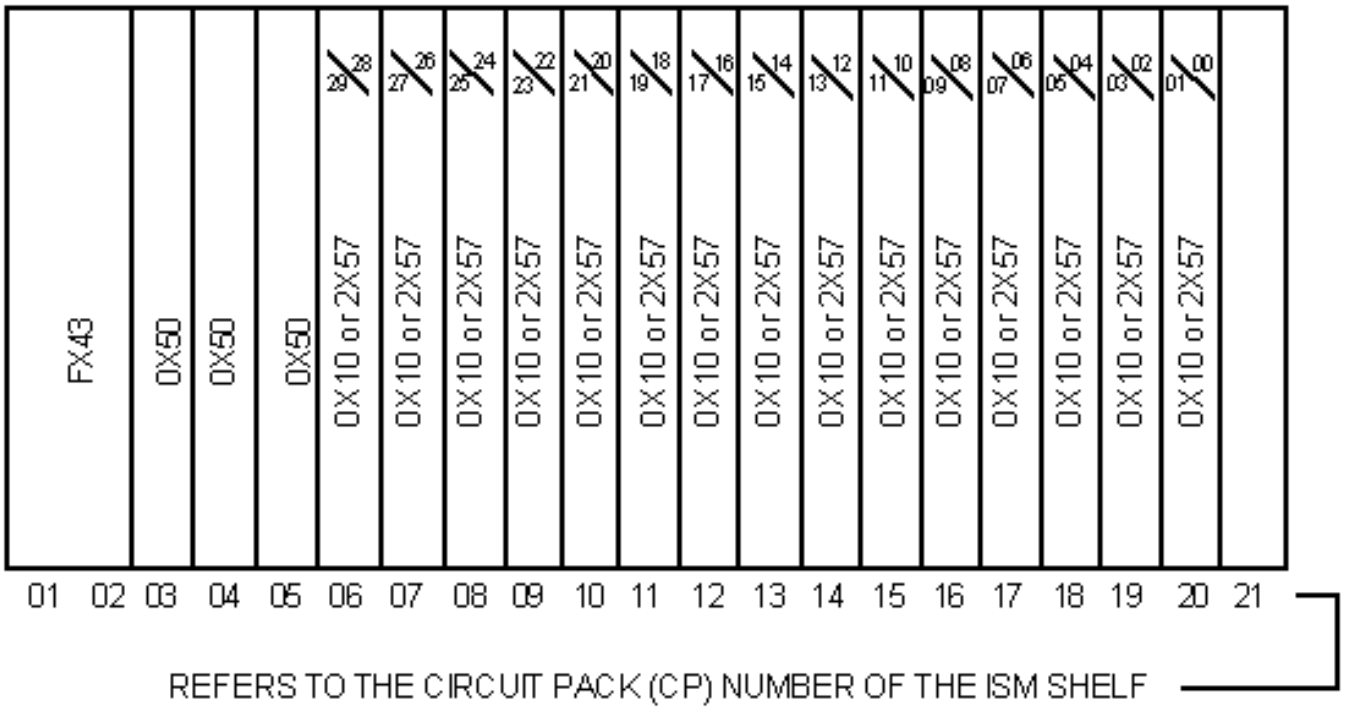


Figure 6•6 Typical Integrated Services Module (ISM) Shelf (NTFX4101)

6.9. DMS-100 SC/SD (INHIBIT) Lead Configuration Testing Architecture 2

Figure 6•7 is an example of the DMS-100 SC/SD (INHIBIT) Lead Configuration Testing Architecture 2.

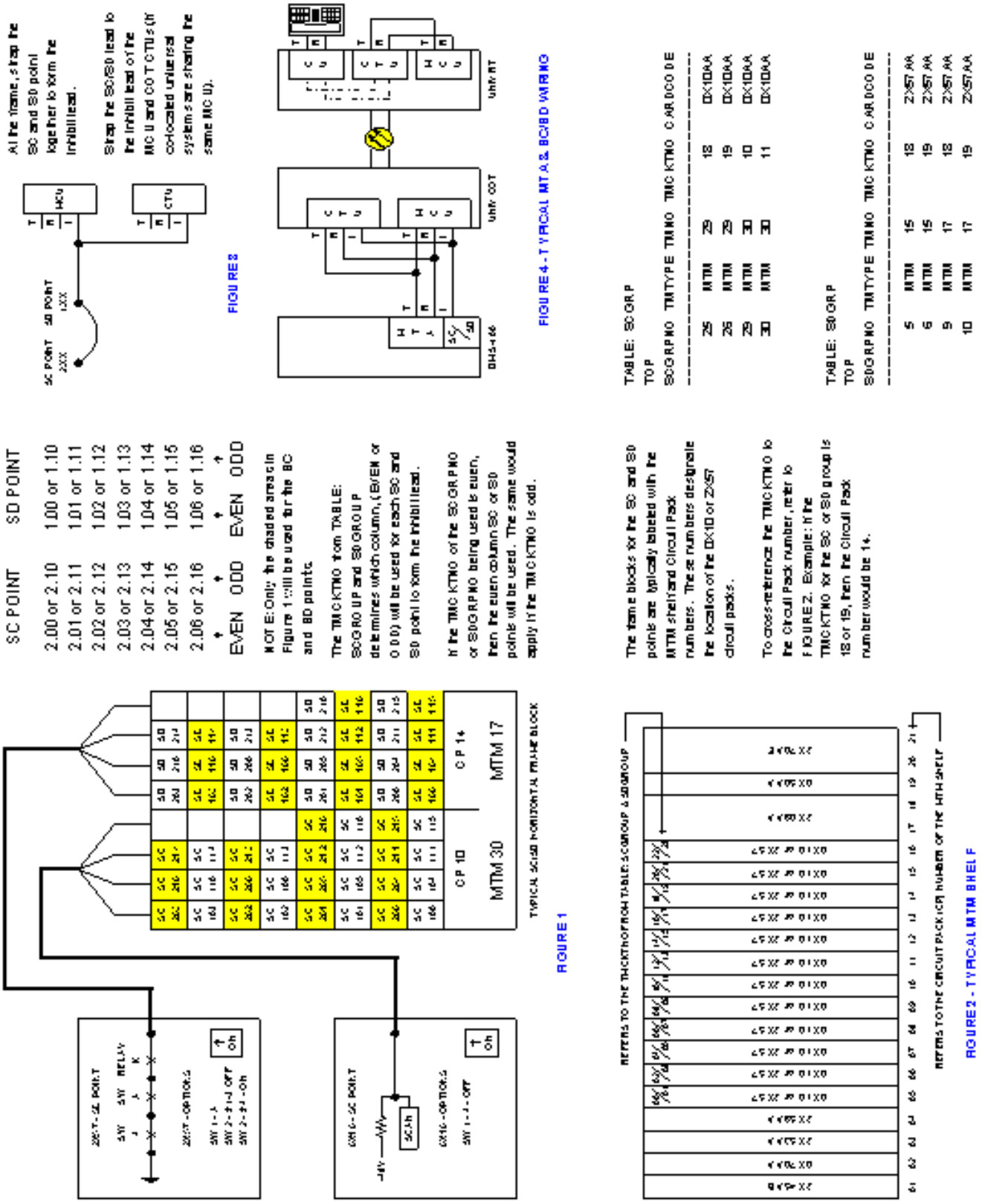


Figure 6•7 DMS-100 SC/SD (INHIBIT) Lead Configuration Architecture 2

6.10. NT0X10 SC Point

Figure 6•8 is an example of a NT0X10 SC Point switch diagram.

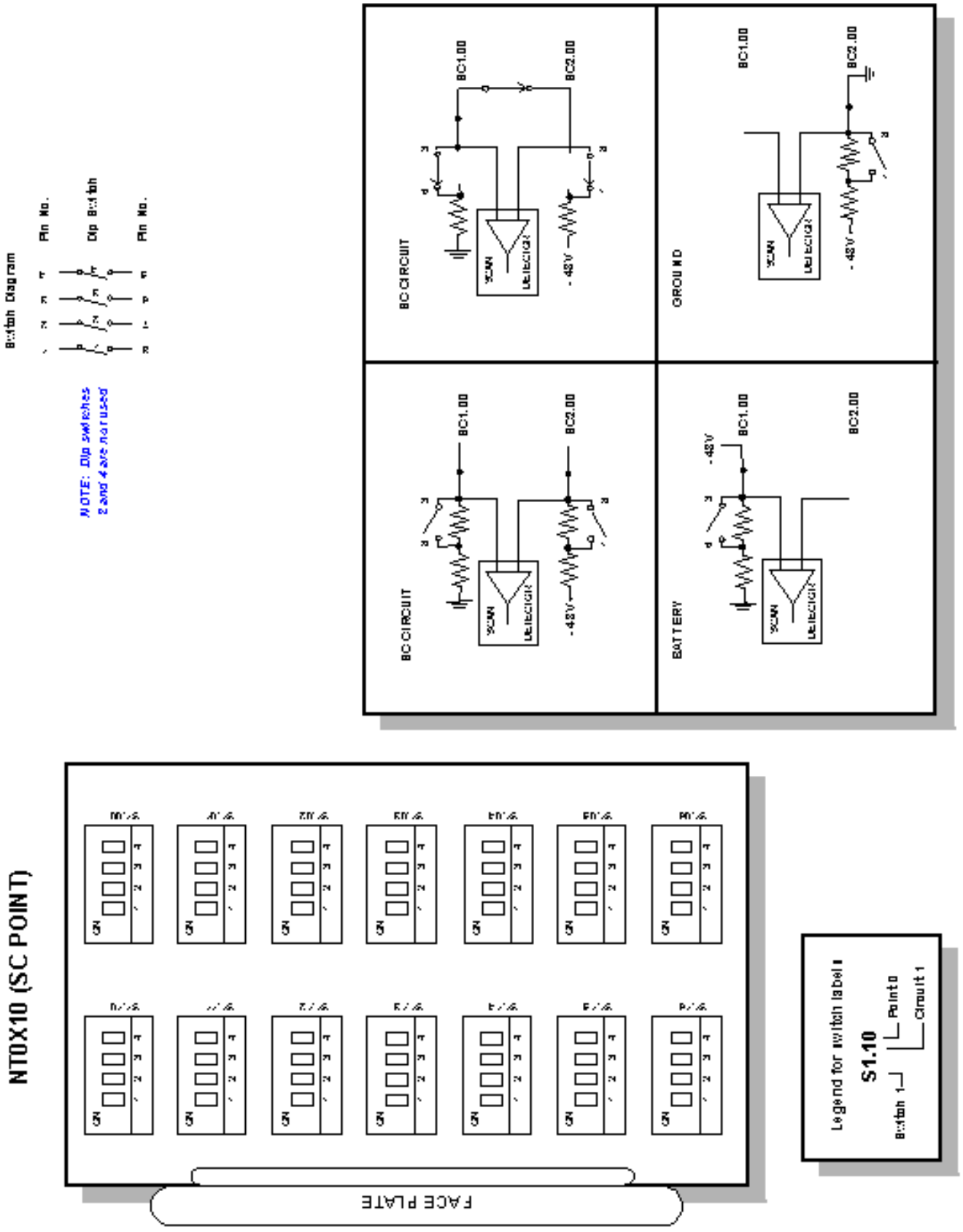
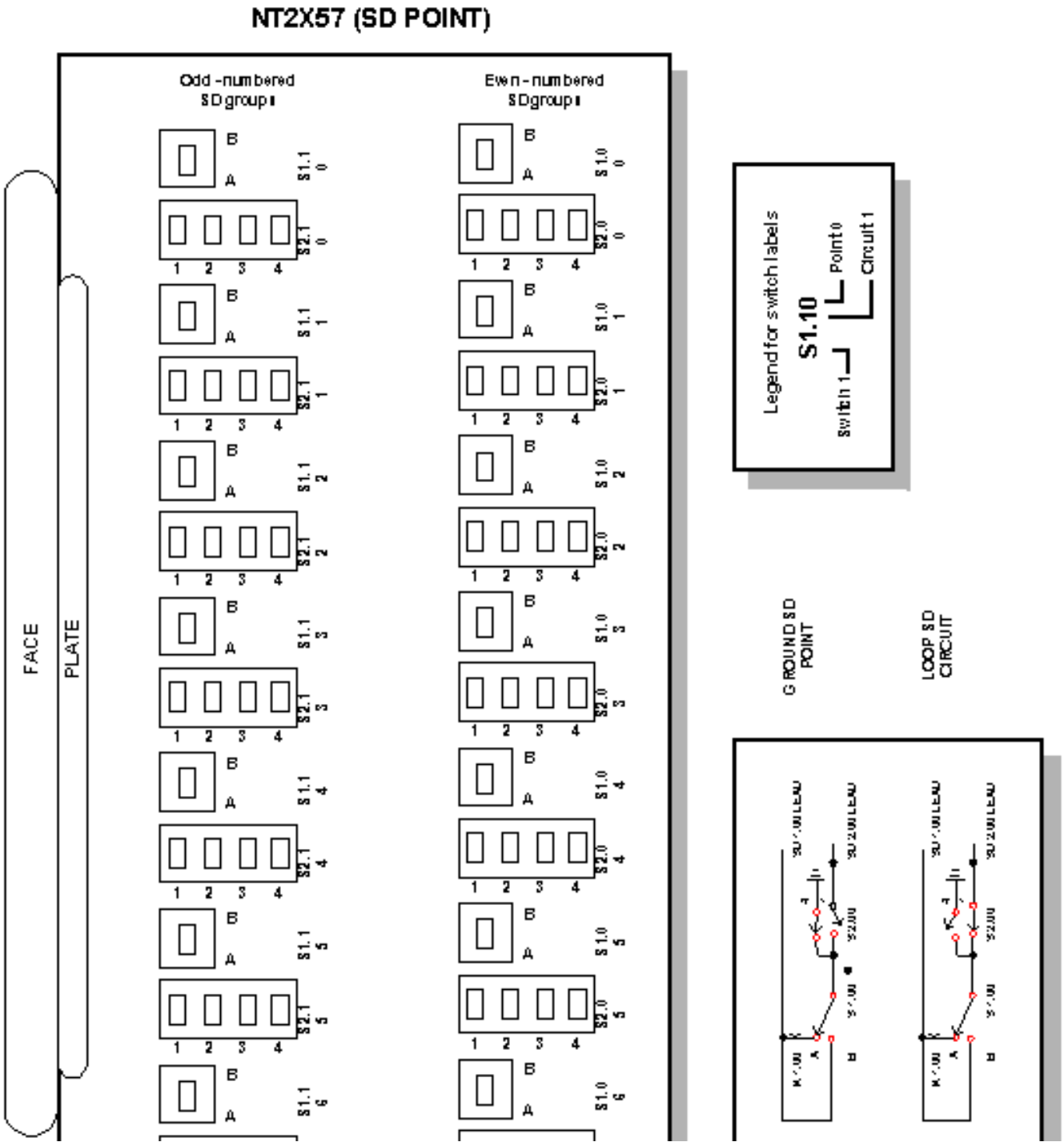


Figure 6•8 NT0X10 SC POINT

6.11. NT2x57 sd Point

Figure 6•9 is an example of a NT2X57 SD Point odd and even numbered groups.



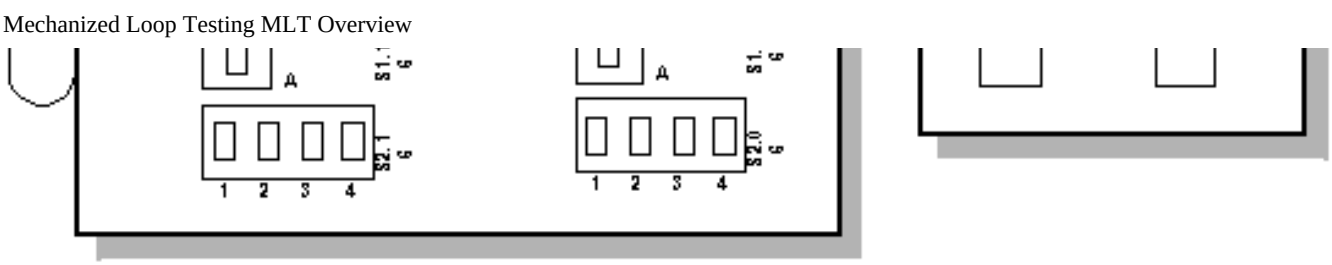


Figure 6•9 NT2X57 SD POINT

6.12. Horizontal and Verticals

Figure 6•10 is an example of a.

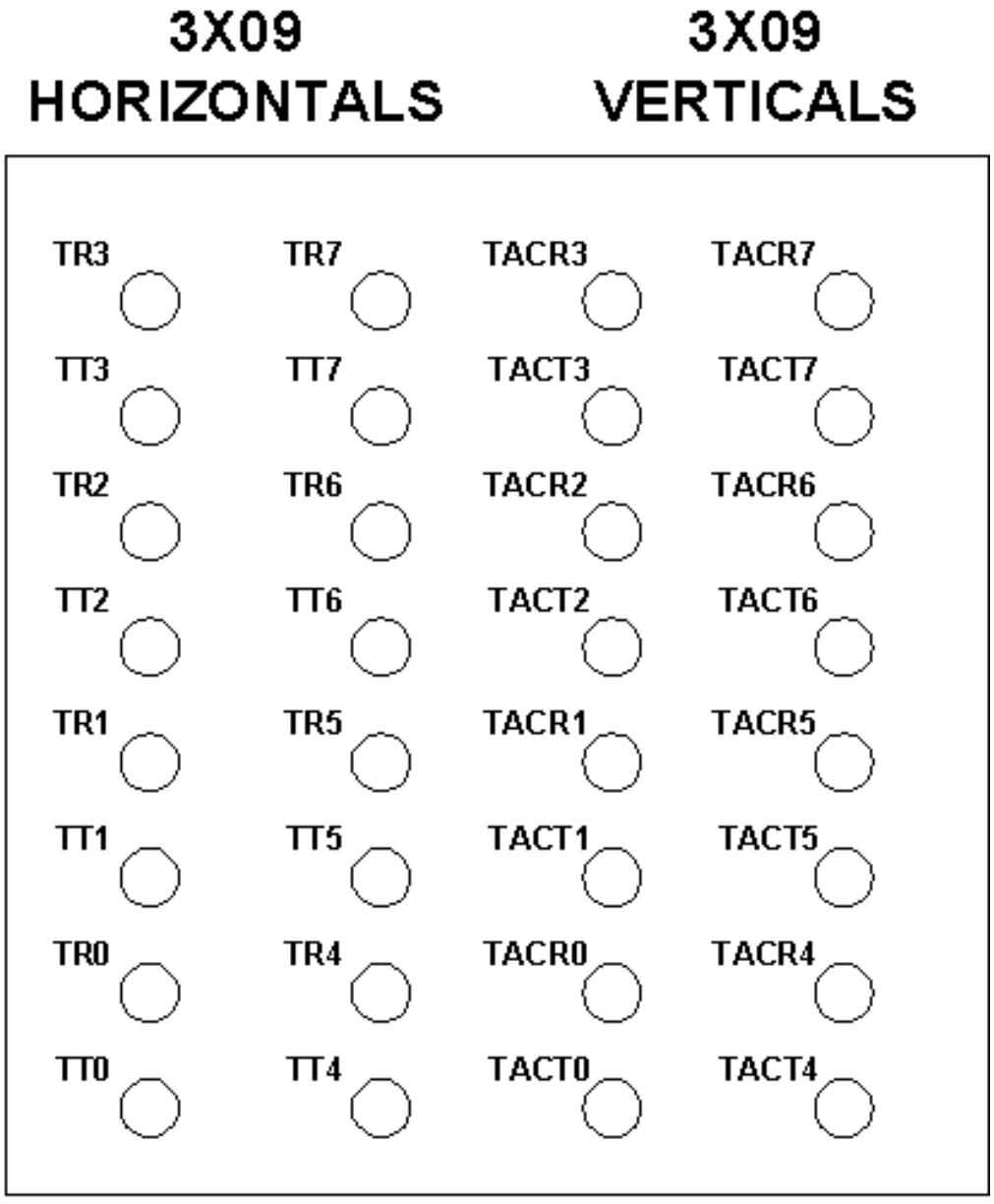


Figure 6•10 Horizontal and Verticals

6.13. Questions

SECTION 7 INTEGRATED DLC TESTING Siemens (EWSD) Switches

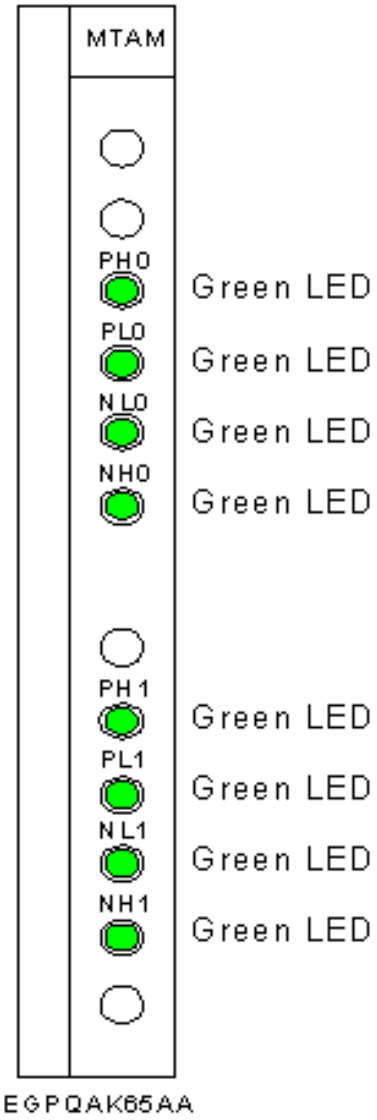
In This Section:

7.1. objectives

The student will understand the hardware and software required for IDLC testing in a Siemens EWSD switch.

7.2. METALLIC TEST ACCESS MODULE (MTAM)

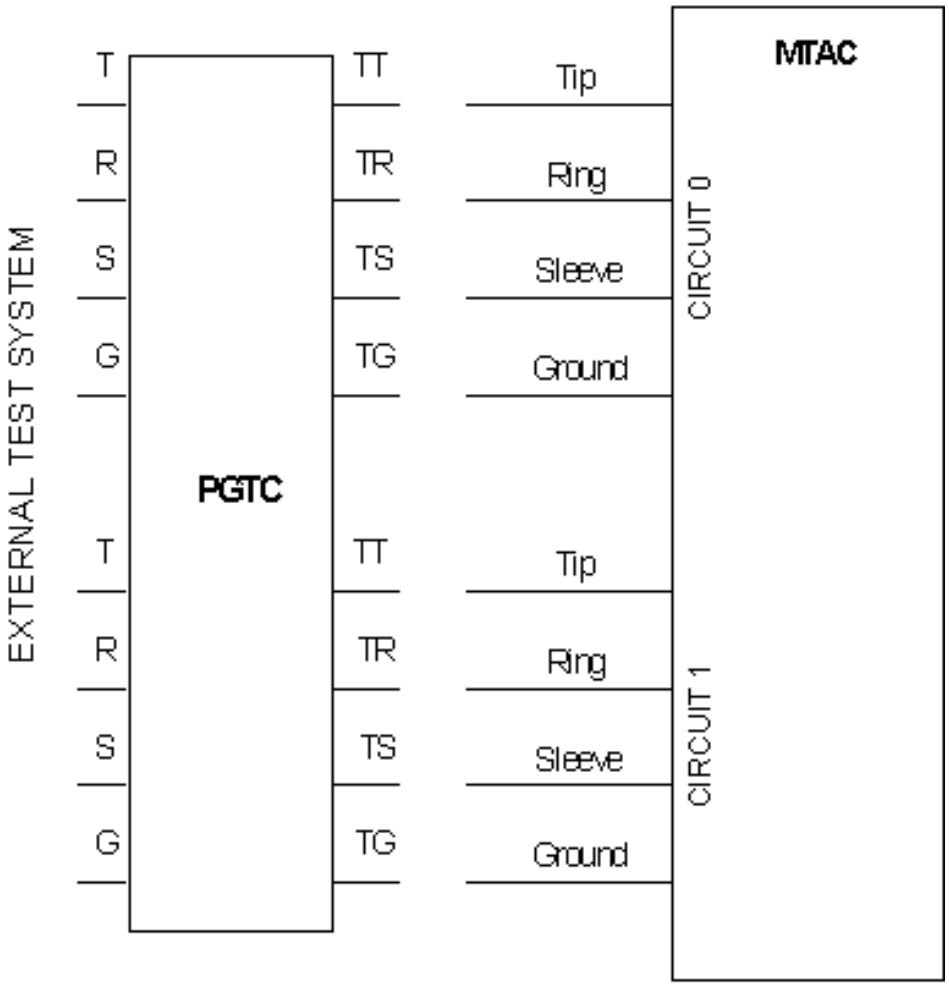
Metallic Test Access Module (MTAM)



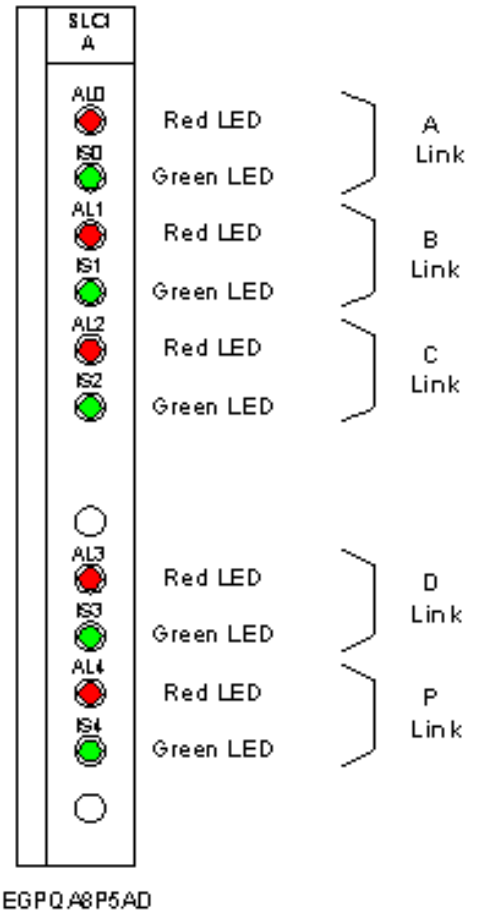
Two sets (**4LEDs/set**), one set per circuit, are provided. They indicate the present status of the sleeve lead circuit. Only the **LED** corresponding to the current state is lit. **See Table 1**

Table 7 Current State and Range

Current State	Current Range(ma)	Sleve Det. Output				LED Output			
		NH	NL	PL	PH	NH	NL	PL	PH
HI POS.	21 to 210	0	0	1	1	0	0	0	1
LOW POS.	6 to 18	0	0	1	0	0	0	1	0
OPEN	+3 to -3	0	0	0	0	0	0	0	0
LOW NEG.	-6 to -18	0	1	0	0	0	1	0	0
HI NEG.	-21 to -210	1	1	0	0	1	0	0	0



7.3. SLC96 INTERFACE MAIN MODULE & SUBMODULE A



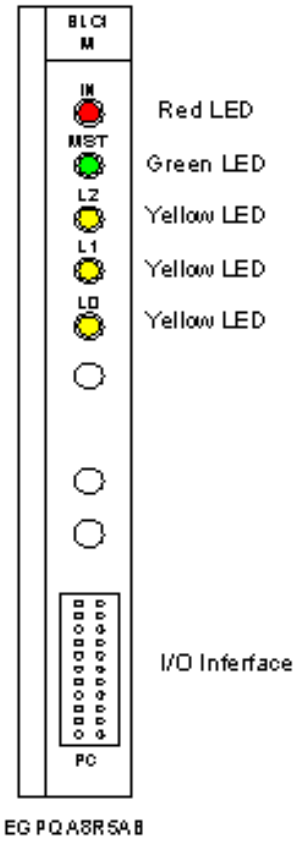
SLC96 Interface Submodule A (SLCIA)

The **SLCI** sub-board (**SLCIA**) contains **2 LEDs** per link. There are a total of **5** links on the **SLCIA** board. There is one red **LED** and one green **LED** to indicate the operational status of the link.

The **LEDs** are controlled by the **SLCI** Maintenance Software and provide status information. **See Table 2**

Table 8 Link Status Indication

LED	State	Link Status Indication
Red	Off	No Major alarm on the link
	On	Major alarm on the link
Green	Off	Link **not** carrying call processing traffic: - In Standby Module - If Link is MBL or PLA - Protection switched to P link - P Link when not protection switched
	On	Link carrying call processing traffic



SLC96 Interface Main Module (SLCIM)

The SLCI main board (SLCIM) contains 5 LEDs which indicate the operational status of the SLCI. **See Table 3**

Table 9 SLCI Status, LED, and Values

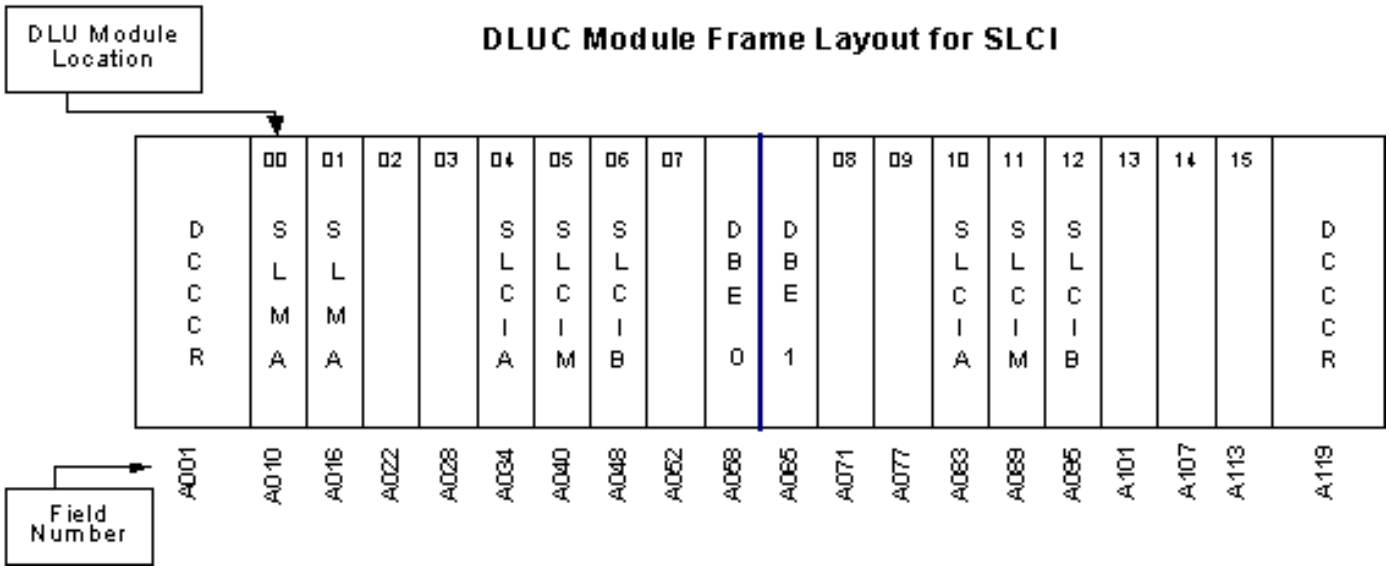
LED	Values	SLCI Status indication
Red	0	Operable (SLCI Processor up)
	1	Inoperable (SLCI) Processor down)
Green	0	Standby SLCI module (no signal asserted on links)
	1	Master SLCI module (signal asserted on links)
Yellow	000	Invalid
	001	Idle / Selftest in BOOT
	010	Download of code in progress
	011	Switchover in progress
	100	Active
	101	Maintenance blocked
	110	Seized by diagnostics
	111	Disturbed

7.4. SLC96 SLCIB and DLUC SLCI

SLC96 Interface Submodule B (SLCIB)

This module interfaces with the **SLCIM** and **SLCIA** modules and is under their control. It provides the following:

- Extends the Metallic Test Bus to the Bypass Pair and the subscriber loops connected to the **SLC-96**.
- Transmits test result voltages to the Line Termination Access (**LTA**).
- Applies **-48 Vdc** to the Ring lead in case of not busy.
- Provides access to the Inhibit lead.



During installation of the **SLCIs**, no more than **18 SLCIBs** (the "**B**" module of the **SLCI**) can be connected to the same **INHIBIT** pair. If this restriction is not adhered to then there will be a problem during line testing. When a test request for a line served by a **SLCI** is made, the **SLCIB** module grounds the **INHIBIT** lead in order to seize the Bypass Pair. At this point the problem occurs: the **50-milliampere** fuse on the **SLCIB**, which lies between the **INHIBIT** lead and the ground relay, opens. The fuse opens because the summation of the currents flowing through the pull-up resistors on each **SLCIB** exceeds the marginal current rating of the fuse. The **INHIBIT** lead is open when the fuse blows, the battery remains on the ring

side of the test pair. **MLT** tests to the affected **RT** site will test **VER 11** or **VER 17** (cross to working pair) **–48 Vdc** on the ring.

7.5. Siemens (EWSD) Switches Serving Alcatel Litespan® Systems

Most Tollgrade customers configure the Alcatel Litespan System for both Universal and Integrated service, plus multiple Remote Terminal (RT) configurations, East and West. The Universal system will use test pair #1, while the Integrated systems may use either test pair #1 or test pair #2, depending on the Interface Group software setting.

The EWSD switch architecture provides for a limit of 18 integrated systems (DLUs) that may share a Metallic Test Path (Tollgrade MCU®-D405). Therefore, a challenge exists when connecting to an Alcatel Litespan DLC with multiple RTs. A solution is spelled out below and depicted on the reverse side of this sheet.

Text Box: Figure 7•1 Tollgrades MCU-D405 Metallic Channel Unit

CONNECTING TO AN ALCATEL LITESPAN DLC WITH MULTIPLE REMOTE TERMINALS

Refer to the drawing on the reverse side of this sheet when following the steps below:

- The East RT has one **MCU-D405 (#1)** installed in CBA #1, configured for the Litespan Mode and wired to the P12 Blue/White pair, by•pass pair #1 IN. Both the Universal and the Integrated systems at **channel (slot)** of the two MCU-D405s at the West RT. MCU-D405 #3 will be wired to the P12 Green/White pair, by-pass pair #2 IN. Only the Integrated systems at the West RT will test using this test path. The Litespan software Interface Groups (IGs) must be set to by-pass pair #2 for all Integrated systems at the West RT.

In the CO, the Integrated system DLUs will be wired together and bridged to the slot

the East RT will test using this test path.

In the Central Office (CO), the Integrated system DLUs will be wired together and bridged to by•pass pair #1 at the UFAP, then wired to the lowest-numbered pairs assigned to the slots for MCU-D405 #1 and MCU-D405 #2. The Inhibit lead of by-pass pair #1 should also be bridged to the Inhibit lead of by•pass pair #2.

- The West RT has two **MCU-D405s (#2 & #3)** installed in CBA #1.

MCU-D405 #2 is configured for the Litespan Mode and installed in the lower-number channel (slot) of the two MCU-D405s at the West RT. MCU-D405 #2 will be wired to the P12 Blue/White pair, by-pass pair #1 IN. Only the Universal systems at the West RT will test using this test path.

MCU-D405 #3 is configured for Normal Industry Mode (Factory Default) and **installed in the higher-number** assigned to MCU-D405 #3. The Tip and Ring will be wired to the lowest pair Tip and Ring. The Inhibit lead will be wired to the Tip of the second-lowest pair.

• This configuration, though a little confusing will ensure good testing for both the Universal and Integrated systems at both the East RT and West RT sites.

• This solution will also work in a 5ESS® or DMS-100® switch.

Note: During installation of the SLCIs, no more than 18 SLCIBs (the "B" module of the SLCI) can be connected to the same INHIBIT pair. If this restriction is not adhered to, then there will be a problem during line testing. When a test request for a line served by a SLCI is made, the SLCIB module grounds the INHIBIT lead in order to seize the by-pass Pair. At this point, the problem occurs: the 50mA fuse on the SLCIB, which lies between the INHIBIT lead and the ground relay, opens. The fuse opens because the sum of the currents flowing through the pull-up resistors on each SLCIB exceeds the marginal current rating of the fuse. The inhibit lead is open when the fuse blows; the

battery remains on the ring side of the test pair. MLT tests to the affected RT site will test VER 11 or VER 17 (cross to working pair) •48 Vdc on the ring.

7.6. SIEMENS SWITCHES SERVING LITESPAN SYSTEMS

Figure 7•2 page 7•8 is an example of the Siemens Switches Serving Litespan Systems.

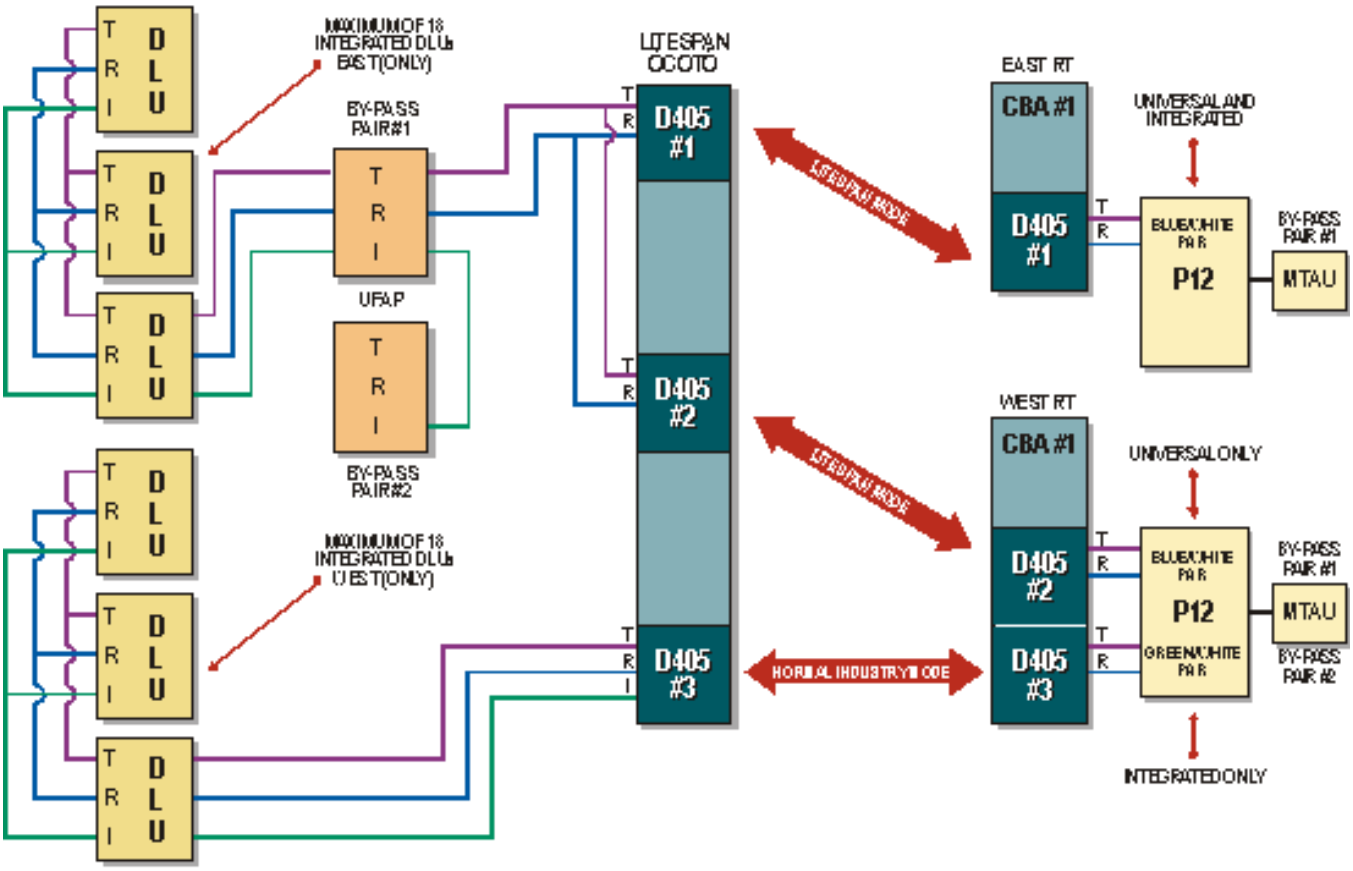


Figure 7•2 Siemens Switches Serving Litespan Systems

7.7. QUESTIONS

1. What DLU leads are used for testing the IDLC?

2. What is the maximum number of DLUs that may be wired together?